ADM-VPX3-9V2
User Manual

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1 Introduction

The ADM-VPX3-9V2 is a 3U VPX embedded high-performance reconfigurable computing card intended for high speed switch applications. Featuring 28G transceivers in the Xilinx Virtex UltraScale+ Plus FPGA at all VPX P1 and P2 wafers, and two FireFly sites for rugged optical communications.

Figure 1 : ADM-VPX3-9V2 Product Photo

1.1 Key Features

Key Features

- PCIe Gen3 x1, x4, x8, or x16 capable
- Convection and conduction thermal management configuration
- 3U, 4HP VPX form factor
- Four banks of DDR4 SDRAM 72 bit wide memory (ECC), 16GB (4GB per bank) rated at 2666MT/s.
- All 32 wafers of P1 and P2 are capable of 28 Gpbs operation (total 896 Gbps)
- 2 FireFly sites each capable of 4x28Gbps operation (total 224 Gbps)
- Option for MPO optical breakout through front panel
- Supports VU9P, VU13P Virtex UltraScale+ FPGAs in the B2104 package
- Debug board fits in 5HP slot profile for easy access to debug switches, LEDs, JTAG, and system monitor
- FPGA configurable over JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring

OpenVPX Compliant Slot Profiles

- SLT3-PAY-2F1F2U-14.2.1
- SLT3-PAY-1F2F2U-14.2.2
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PAY-1F1U-14.2.10
- SLT3-PAY-2F4F2U-14.2.11
- SLT3-PAY-1F2U-14.2.12
- SLT3-PAY-3F2U-14.2.13
- SLT3-PAY-2U2U-14.2.17
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3
- SLT3-PER-1Q-14.3.4
- SLT3-SWH-6F6U-14.4.1
- SLT3-SWH-8F-14.4.2
- SLT3-SWH-2F24U-14.4.3
- SLT3-SWH-4F-14.4.4
- SLT3-SWH-2F8U-14.4.5
- SLT3-SWH-6F8U-14.4.9
- SLT3-SWH-6F8U-14.4.9

1.2 Order Code

See http://www.alpha-data.com/pdfs/adm-vpx3-9v2.pdf for complete ordering options.

2 Board Information

2.1 Physical Specifications

The ADM-VPX3-9V2 complies with 4HP pitch slot profiles from AV48.1 and AV48.2 respectively

Description	Measure
Total Dy	100 mm
PCB Dy	94 mm
Total Dx	171 mm
PCB Dx	160 mm
Total Dz	21.5 mm
Weight (no heat sink)	180g

Table 1 : Mechanical Dimensions

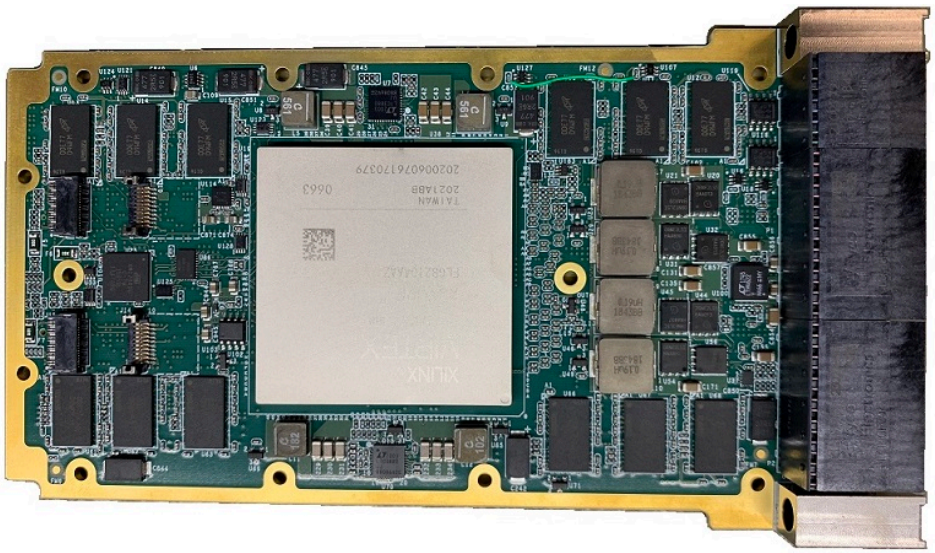

Figure 2 : ADM-VPX3-9V2 Top View

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-VPX3-9V2 is capable of PCIe Gen 3 with up to 16 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

A 3U VPX compliant backplane is required for use with this module.

2.2.3 Power Requirements

The ADM-VPX3-9V2 draws power from only VS1 (12V) and the 3.3V auxiliary power. All other power rails are unused and unconnected.

Power consumption estimation requires the use of the Xilinx XPE spreadsheet and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85-0.90	VCC_INT + VCCINT_IO + VCC_BRAM	105A
0.9	MGTAVCC	7A
1.2	MGTAVTT	12A
1.2	1V2_DIG (DDR4)	12A
1.8	VCCAUX + VCCAUX_IO + VCCO_1.8V	5.5A
1.8	MGTVCCAUX	1A
3.3	3.3V (FireFly and logic ICs)	5A

Table 2 : Available Power By Rail

2.3 Thermal Performance

If the FPGA core temperature exceeds 105 degrees Celsius, the FPGA design will be cleared to prevent the card from over-heating.

The ADM-VPX3-9V2 comes with either a convection or conduction heat sink. The only part of the card monitored for over-temperature shutdown is the FPGA, since it is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius. To calculate the FPGA die temperature in a convection application, take your application power, multiply by Theta JA from the table below, and add to your system internal ambient temperature. Conduction cards typically perform with a constant theta JC (chassis wall) of 0.4 degC/W.
This thermal efficiency translates to the following thermal profiles:
- AV47 CC2 (-40°C 55°C) with a maximum 112W design
- AV47 CC3 (-40°C 70°C) with a maximum 75W design
- AV47 CC4 (-40°C 85°C) with a maximum 37W design

Real time power measurements can be taken from the system monitor 12V voltage and current values. See System Monitor for more details.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the device to Virtex UltraScale+, VU9P or VU13P, B2104 package, -2, Industrial. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next, acquire the 9V2 power estimator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures to get a board level estimate.

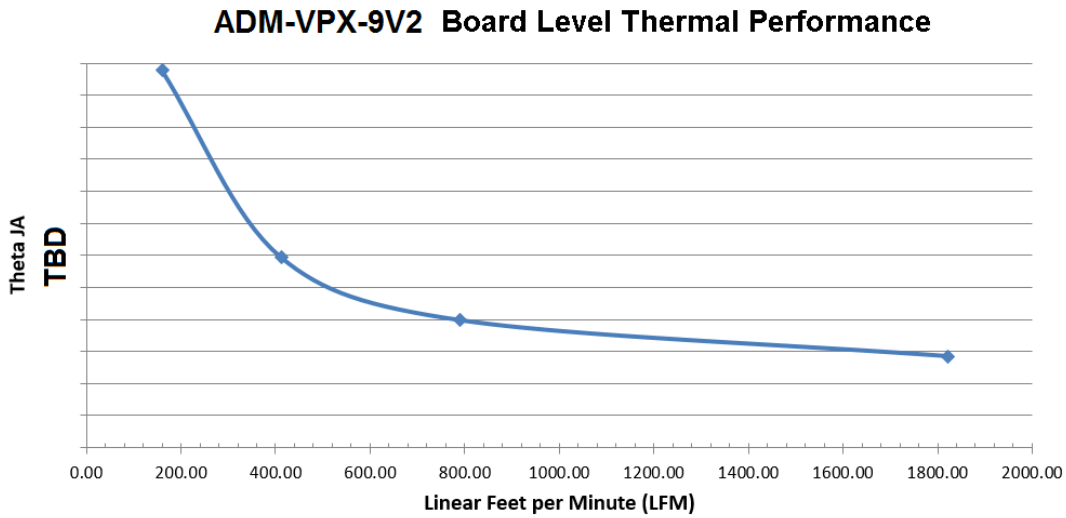

Figure 3 : Thermal Performance

2.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: custom Front IO, enhanced heat sinks, alternate FPGA part number support, and circuit additions.

See https://www.alpha-data.com/mcots.php for more details.

3 Functional Description

3.1 Overview

The ADM-VPX3-9V2 is a versatile reconfigurable computing platform with a Virtex UltraScale+ VU9P/VU13P FPGA, 32 reconfigurable VPX lanes and 8 FireFly lanes all capable of 28G/lane, and four banks of 72 bits wide (for 64 bits with 8 bits ECC) DDR4 memory. The 9V2 also comes with a compact debug board with LEDs, switch, programming headers, and easy access to the powerful onboard system monitor features.

The ADM-VPX3-9V2 comes with a front access debug board which includes: 8 user LEDs, 4 status LEDs, DIP switch, Xilinx JTAG programing header, micro usb access to system montior, and factory programing headers.

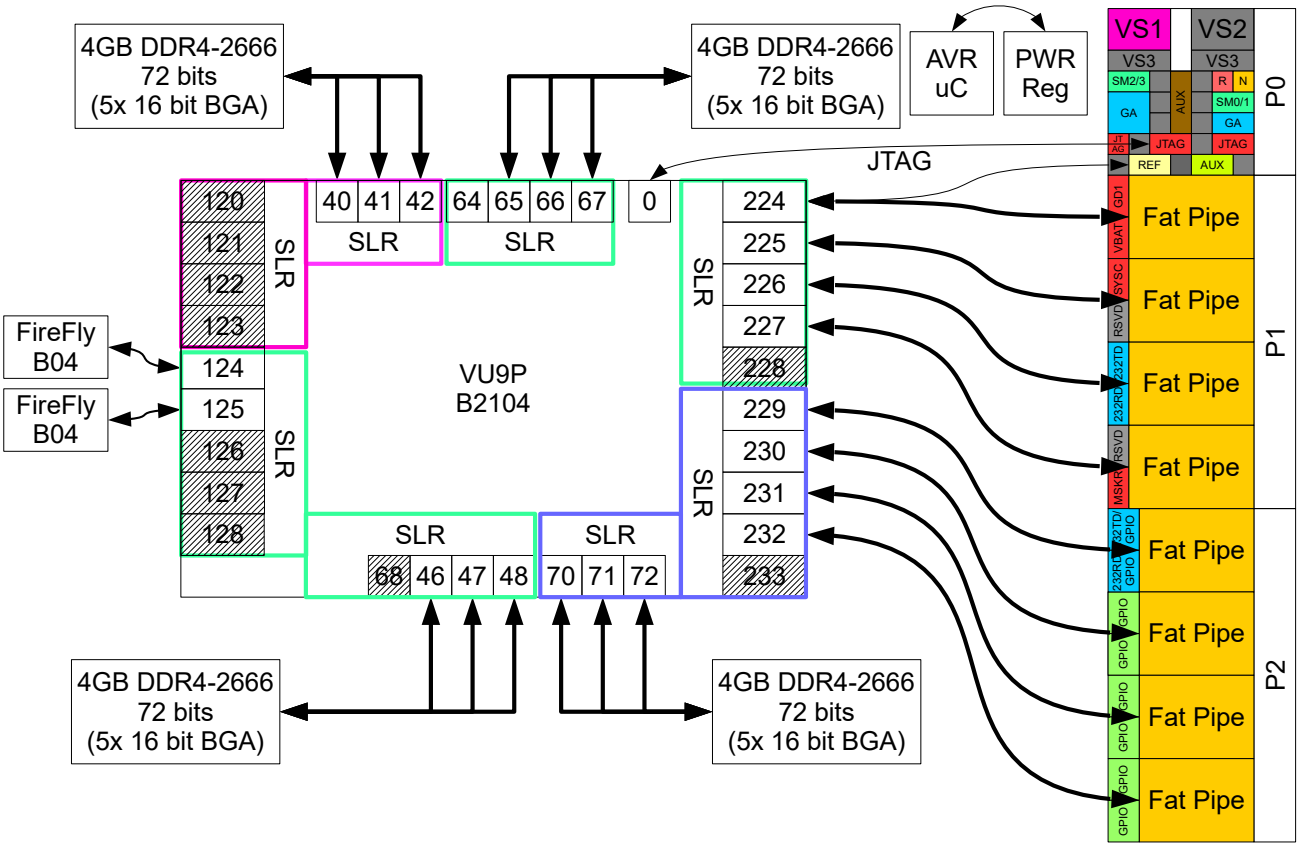

Figure 4 : ADM-VPX3-9V2 VU9P Block Diagram

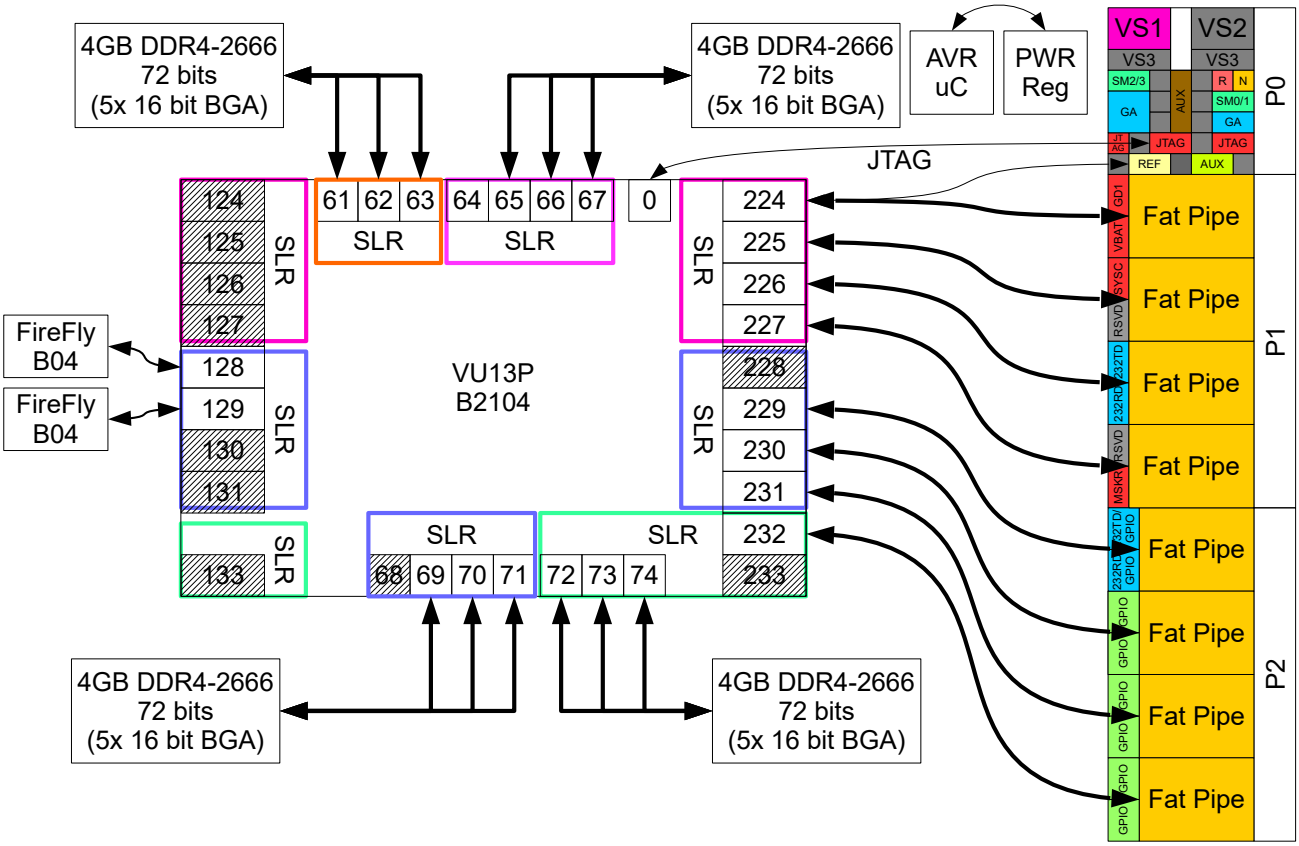

Figure 5 : ADM-VPX3-9V2 VU13P Block Diagram

Figure 6 : ADM-VPX3-9V2 with debug board

3.1.1 Switches

The ADM-VPX3-9V2 has a quad DIP switch SW1, located on the debug board. The function of each switch in SW1 is detailed below:

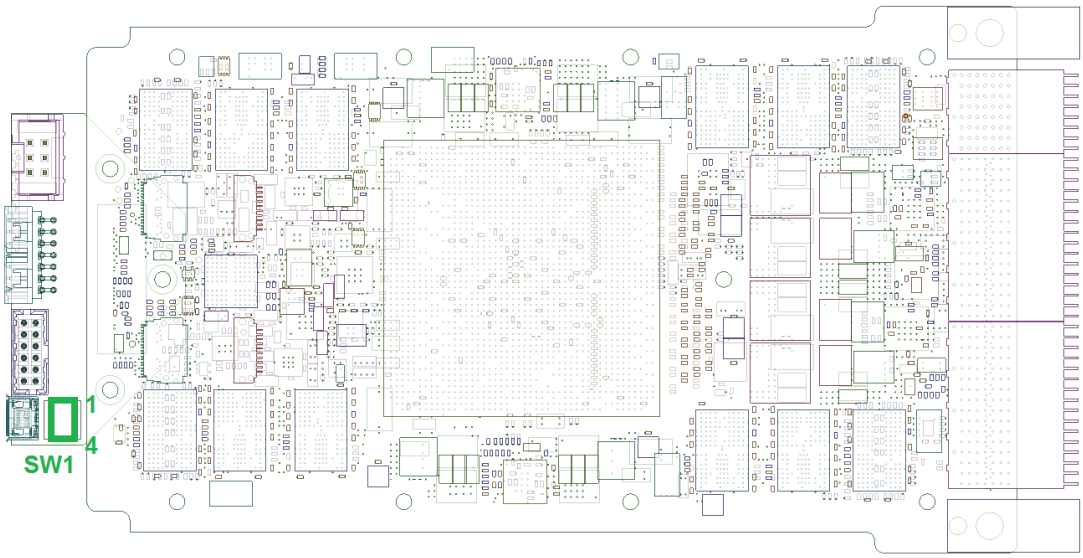

Figure 7 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch 0	Net DBG_USER_IN_0 = '1'	Net DBG_USER_IN_0 = '0'
SW1-2	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW1-3	OFF	CLK_SEL	Board synchronizes to onboard 25MHz	Board synchronizes to VPX REFCLK 25MHz
SW1-4	OFF	Power Off	Board will power up	Immediately power down

Table 3 : Switch Functions

See Section Complete Pinout Table for full list of user controlled switch nets and pins

3.1.2 LEDs

There are 12 LEDs on the ADM-VPX3-9V2 debug board, 8 of which are general purpose and whose meaning can be defined by the user. These user LEDs do not have a default value, and could be in any state when the FPGA is unconfigured, or these pins are unconstrained (i.e. they may be on/off/flickering). The other 4 have fixed functions described below:

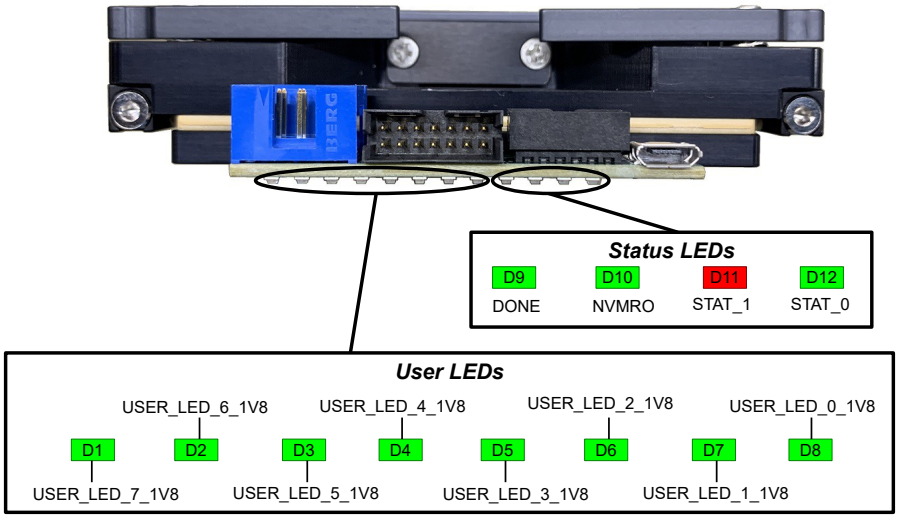

Figure 8 : Front Panel LEDs

Comp. Ref.	Function / Net Name	ON State	OFF State
D8	USER_LED_0_1V8	User defined '0'	User defined '1'
D7	USER_LED_1_1V8	User defined '0'	User defined '1'
D6	USER_LED_2_1V8	User defined '0'	User defined '1'
D5	USER_LED_3_1V8	User defined '0'	User defined '1'
D4	USER_LED_4_1V8	User defined '0'	User defined '1'
D3	USER_LED_5_1V8	User defined '0'	User defined '1'
D2	USER_LED_6_1V8	User defined '0'	User defined '1'
D1	USER_LED_7_1V8	User defined '0'	User defined '1'
D9	DONE	FPGA is configured	FPGA is not configured
D10	NVMRO_L	NVMRO signal active	NVMRO signal inactive
D11	Status 1	See Status LED Definitions	
D12	Status 0	See Status LED Definitions	

Table 4 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 VPX P0

3.2.1 Global Address

All global address pins are available as inputs to the FPGA.

See net names FPGA_GA* in section Complete Pinout Table for location details.

3.2.2 System Reset

SYSRESET# provides an input to the FPGA at the dedicated PERSTN0 pin for use with PCIe or general resets.

SYSRESET# can also be driven through an open drain buffer by the FPGA at net SYSRESET_OUT_L which can be located in the section Complete Pinout Table.

3.2.3 REFCLK

VPX REFCLK is an optional VPX input/output that should be either a 25MHz or a 100MHz reference clock. By default this clock is forwarded to MGTREFCLK0 of quad 224.

When REFCLK is 25MHz, it can be used as the clock source for all internally generated clocks. This is done by setting SW1-3 on the debug board to ON, or through a build option.

The net REFCLK_OUT_EN_1V8 when driven high, will change the external REFCLK transceiver into an output driver, and forward the net SE_REFCLK_OUT_1V8 onto the VPX backplane.

See net names in section Complete Pinout Table for location details.

3.2.4 AUXCLK

VPX AUXCLK is an optional VPX input/output that can provide an external reference timing pulse or clock. By default this clock is forwarded as net name AUXCLK_SE_1V8 GPIO in FPGA bank 64.

The net AUXCLK_DIR_1V8 when driven high, will change the external AUXCLK transceiver into an output driver, and forward the net AUXCLK_SE_1V8 onto the VPX backplane.

See net names in section Complete Pinout Table for location details.

3.2.5 Management Bus (SM0-SM3)

The default build option sends SM0-SM3 to the FPGA for user implementation at net locations IPMB0_FPGA_SCL, IPMB0_FPGA_SDA, IPMB1_FPGA_SCL, IPMB1_FPGA_SDA found in Complete Pinout Table.

SM0-SM3 are buffered through a LTC4309IDE I2C bus level translator to ensure high impedance isolation during partial power-down.

SM0-SM3 can be controlled by the onboard system management microcontroller, but this requires a small resistor population change controlled by a build modification.

See net names in section Complete Pinout Table for location details.

3.2.6 NVMRO

NVMRO is available as an input at net NVMRO_FPGA.

NVMRO can also be connected to the configuration flash memory through a build option upon request. Note that this will increase the power-on configuration time for the FPGA by a factor of 2.

See net names in section Complete Pinout Table for location details.

3.3 VPX P1 and P2

3.3.1 Differential Pairs

All differential wafers in P1 and P2 are connected directly to high speed transceivers on the FPGA. These connectors use RT3 VPX connectors which are capable of up to 28Gbps line rates. The FPGA is very flexible, and these 32 lanes can be configured as any combination of 32 ultra-thin-pipes, 16 thin-pipes, 8 fat-pipes, or 4 ultra-fat-pipes as defined in the VPX specifications. These wafers can support protocols like 100G ethernets, SRIO, Infiniband, or any other protocol supported directly by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All VPX differential lines (both RX and TX) have 220nF AC coupling capacitors in line for the most flexibility. Alpha Data can change the value of these capacitors, or change them to 0 ohm resistors upon request.

See Overview for quad and wafer mapping. Net nomenclature is shown below:
Wafer connections

- P1 Wafers 1-8: PCIE_*
- P1 Wafers 9-14: P1_*
- P1 Wafer 15: ETH2_*
- P1 Wafer 16: ETH1_*
- P2 Wafers 1-16: P2_*

See net names in section Complete Pinout Table for location details.

3.3.2 P1 GDISC1#

GDiscrete1 is an optional, bidirectional, open drain, IO pin defined in the VPX specification at P1 pin G1. It is controlled at the FPGA by net GDiscrete1_OUT and GDiscrete1_IN, both of which have external pull-ups. An external open-drain buffer passes and receives logical low signals from the shared backplane bus to the FPGA.

Locations for these net names can be located in section Complete Pinout Table.

3.3.3 VBAT

VBAT is connected through a resistor divider to the FPGA VBAT pin, and can provide voltage to hold encryption keys for secure boot load.

3.3.4 SYSCON#

The system controller input is buffered and sent to the FPGA as net SYSCON_1V8_L. The ADM-VPX3-9V2 has some system controller functionality build in (REFCLK, management bus flexibility, SYSRESET control, etc.), and can perform this function in some chassis.

3.3.5 MP01

The OpenVPX MP01 serial port at P1.G9 and P1.G11 is configurable as either 3.3V UART (default) or optionally RS232 signaling levels (with build option). See net names UART_0_* and RS232_0 in Complete Pinout Table for pin locations.

3.3.6 AX_RESETL#

This input is unused by default, and requires a build option to use this signal.

3.3.7 MSKRST#

The VPX maskable reset is combined with the system reset and sent to the dedicated PERSTN0 pin of the FPGA. This is an ideal way to perform PCIe reset, or general logic resets.

3.3.8 P2 GPIO

All 8 user defined pins on row G of P2 are controllable through an SN74AVC4T774RSVR bidirectional buffer with an external pull-up. The buffers are enabled with active low net P2_GPIO_EN_L (there is an external pull-up). Each line has a directional control pin P2_GPIO_G*_DIR. DIR set high drives a GPIO out onto the backplane, and logical low receives in from the backplane (there is an external pull-down). Nets P2_GPIO_*_1V8 are the input/output pins to send and receive data.

MP02 at P1 pins G1 and G3 can be used as a serial 3.3V UART interface as per OpenVPX when configured with the appropriate input and output directions.

Locations for these net names can be located in section Complete Pinout Table.

3.3.9 MP02

The OpenVPX MP02 serial port at P2.G1 and P2.G3 is configurable as either 3.3V UART (default) or optionally RS232 signaling levels (with build option). See net names GPIO_G1_1V8, GPIO_G3_1V8, and RS232_1* in Complete Pinout Table for pin locations.

3.4 Clocking

The ADM-VPX3-9V2 provides flexible reference clock solutions for the many multi-gigabit transceiver quads and FPGA fabric. Any programmable clock, from the SI5338 Clock Synthesizer, is re-configurable from the debug board USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency is 312.5MHz. Customers who utilize Alpha Data SDK and API also have the option of embedding IP into their FPGA design that permits programmable clock re-configuration via PCIe or from within the FPGA.

All clock names in the section below can be found in Complete Pinout Table.

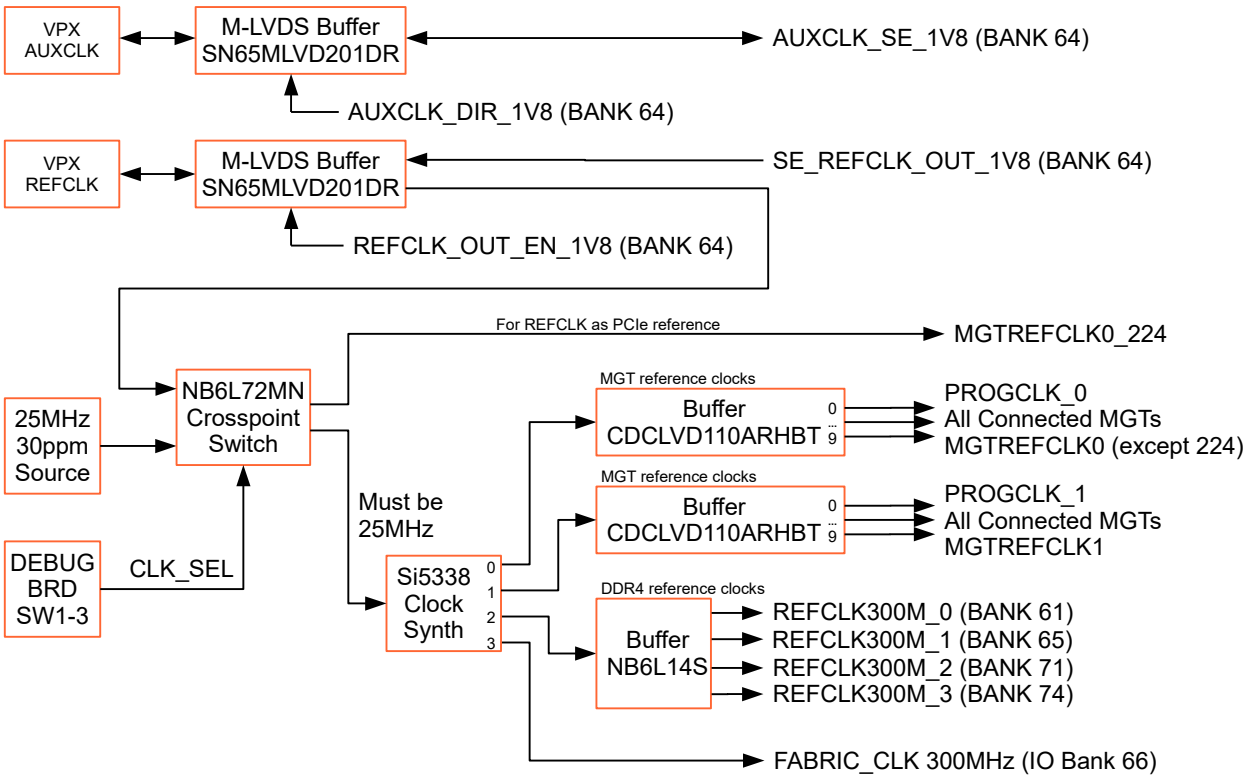

Figure 9 : Clock Topology

3.4.1 PCIe Reference Clock

Quad 224 can serve as an input for the PCIe reference clock. This quad has direct access to VPX REFCLK at MGTREFCLK0. Any other suitable quad can provide a PCIE reference clock with PROGCLK0* or PROGCLK1* as well.

3.4.2 Fabric Clock

The design offers a fabric clock (net name FABRIC_CLK_*) which defaults to 300 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin.

DIFF_TERM_ADV = TERM_100 is required for LVDS termination

3.4.3 Programming Clock (EMCCLK)

A 100MHz clock (net name EMCCLK_B) is fed into the EMCCLK pin to drive the SPI flash device during configuration of the FPGA. Note that this is not a global clock capable IO pin.

3.4.4 PROGCLK0 Clock

The PROGCLK_0 clocks have a default 100MHz reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

The PROGCLK_0 connects at each usable MGT quad at the MGTREFCLK0 location. Quad 224 is the only exception, which is connected to VPX REFCLK instead. PROGCLK0_9* is connected to global clock pins at Bank 68 as well.

See net names PROGCLK_0* for pin locations.

3.4.5 PROGCLK1 Clock

The PROGCLK_1 clocks have a default 156.25MHz reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

The PROGCLK_1 connects at each usable MGT quad at the MGTREFCLK1 location.

See net names PROGCLK_1* for pin locations.

3.4.6 DDR4 SDRAM Reference Clocks

The four banks of DDR4 SDRAM memory each receive a separate reference clock, as per Xilinx UltraScale MIG design guidelines. The reference clocks for these interfaces are nets beginning with REFCLK300M*.

The default frequency is 300MHz. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

3.5 PCI Express

The ADM-VPX3-9V2 is capable of PCIe Gen 3 between 1 and 16 lanes. The FPGA drives these lanes dirctly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) dedicated reset pin on the FPGA (IO_T3U_N12_PERSTN0_65) is driven by either/or VPX system reset or the slot maskable reset. Complete Pinout Table signal PERSTN0.

The other pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table

The PCI Express specification requires that all add-in cards be ready for enumeration within 120ms after power is valid (100ms after power is valid + 20ms after PERST is released). The ADM-VPX3-9V2 does not meet this requirement, but will configure in about 200ms when configured from a tandem bitstream with the proper SPI constraints detailed in the llink:section:Configuration From Flash Memory. For more details on tandem configuration, see Xilinx XAPP 1179.

Note:
Different SBCs/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by Xilinx. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" from "Add-in Card" to "Chip-to-Chip" (See Xilinx PG195, PG213, and PG239 for more details).

3.6 FireFly

A Samtec FireFly site located near the front of the board allows for additional high speed optical or copper cabled links running at up to 224G total (2 ports with 4 channels at up to 28G).

More details on FireFly can be found at https://www.samtec.com/optics/optical-cable/mid-board/firefly

It is possible for Alpha Data to pre-fit industrial or commercial optical FireFly modules. Please contact sales@alpha-data.com for full details and options.

FireFly optical modules are robust to mechanical shock up to 11 ms / 20 g peak saw tooth shock and random vibration to a level of W0 = 0.061 g2/Hz, per MIL-STD-810G.

All connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the net names is FIREFLY_0*, FIREFLY_1*.

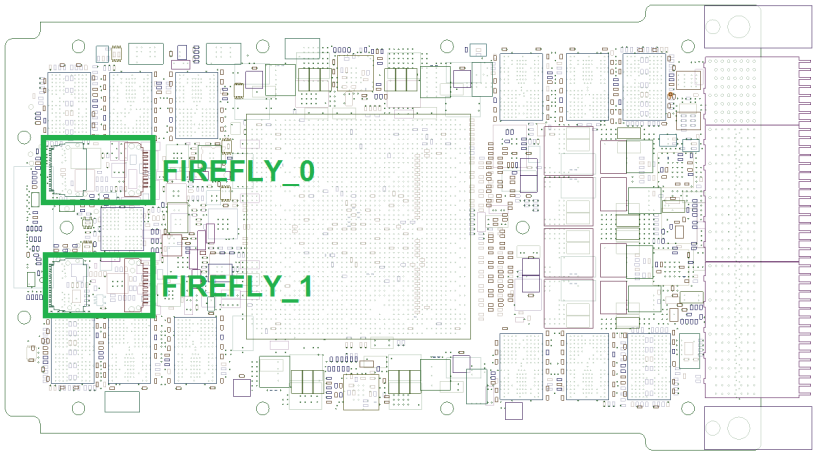

Figure 10 : FireFly Location

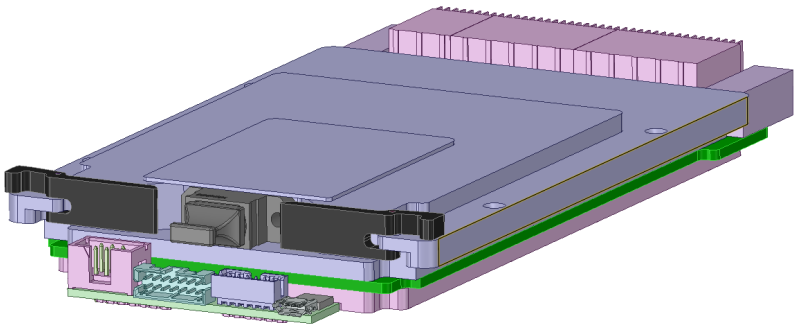

Figure 11 : MPO with Conduction Cooled

3.7 DDR4 SDRAM

four banks of DDR4 SDRAM memory are soldered down to the board. The available density of the memory is 4GB/per bank, 16GB total. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 2666 MT/s.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. An example memory exerciser project is included in the ADM-VPX3-9V2 SDK. All constraint information is included in Complete Pinout Table.

The 8Gb components used are Micron MT40A512M16LY-062E IT

The DDR4 ICs are placed and routed with the clamshell topology. Ensure the "clamshell" check box in the MIG IP tools is selected to enable proper address control.

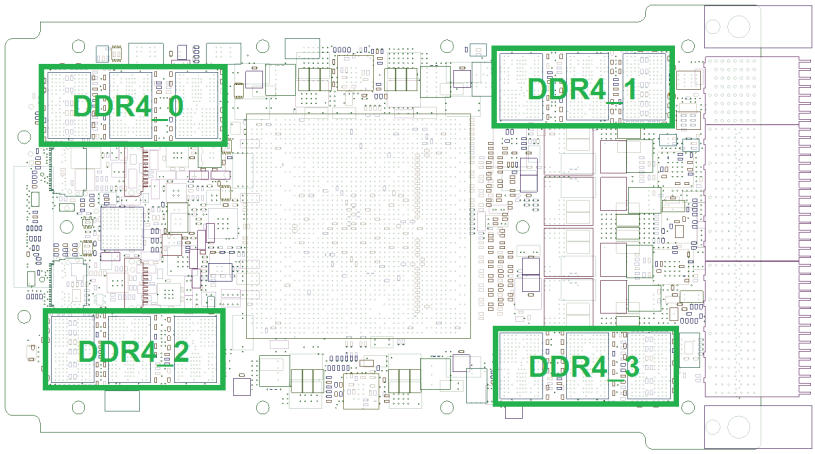

Figure 12 : DDR4 bank locations by index

3.8 System Monitor

The ADM-VPX3-9V2 has the ability to monitor its own temperature, voltages, and currents of certain power supply rails. These metrics provide an indication of board health. The monitoring is implemented using an Atmel AVR microcontroller.

If the core FPGA temperature exceeds 105 degrees Celsius, the FPGA will be cleared to prevent damage to the card.

The microcontroller monitors can be read out via USB using the avr2util utility, and also via PCIe using the Alpha Data Board Support Package (BSP).

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V0_DIG	ADC00	12V board input supply from VS1
12V0_DIG_I	ADC01	12V input current from VS1 in amps
3V3_AUX	ADC02	3.3V auxiliary board input supply from PCIE edge
3V3_DIG	ADC03	3.3V generated onboard for QSFP optics
2V5_DIG	ADC04	2.5V generated onboard for DRAM
2V5_CLK	ADC05	2.5V generated onboard for clock circuitry
1V8_DIG	ADC06	1.8V generated onboard for FPGA IO voltage (VCCO)
1V8_MGT_AUX	ADC07	1.8V generated onboard for transceiver power (AVCC_AUX)
1V2_DIG	ADC8	1.2V generated onboard for DDR4 (VCCO)
1V2_AVTT	ADC9	1.2V generated onboard for transceiver Power (AVTT)
0V9_AVCC	ADC10	0.9V generated onboard for transceiver Power (AVCC)
0V85_DIG	ADC11	0.85V generated onboard for FPGA core (VCCINT)
0V6_DRAM_VTT_1	ADC12	0.6V generated onboard for DDR4 termination
0V6_DRAM_VTT_0	ADC13	0.6V generated onboard for DDR4 termination
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature near rail (U3)
Board1_Temp	TMP02	Board temperature near opposite rail (U23)
FPGA_Temp	TMP03	FPGA on-die temperature

Table 5 : Voltage, Current, and Temperature Monitors

3.8.1 System Monitor Status LEDs

LEDs D11 (Red) and D12 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 6 : Status LED Definitions

3.9 USB Interface

The USB connector on the debug board is used to directly access the system monitor. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.

For example "avr2util.exe /usbcom com4 display-sensors" will display all sensor values.

For example "avr2util.exe /usbcom com4 setclknv 1 100000000" will set the PROGCLK_1 to 100MHz. setclk index 0 = PROGCLK_0, index 1 = PROGCLK_1, index 2 = REFCLK300 (DRAM), index 3 = FABRIC_CLK.

Change 'com4' to match the com port number assigned under windows device manager.

3.10 Configuration

There are two main ways of configuring the FPGA on the ADM-VPX3-9V2:

- From Flash memory, at power-on, as described in Section 3.10.1
- Using JTAG at either the debug board or P0 Section 3.10.2

3.10.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from one 2 Gbit QSPI flash memory device configured as an x4 SPI device (Micron part numbers MT25QU02GCBB8E12-0). These flash devices are typically divided into two regions of 128 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU9P or VU13P FPGA.

The ADM-VPX3-9V2 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using e.g. Windows Device Manager or “lspci” in Linux) in order to provided confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact sales@alpha-data.com in order to discuss this possibility.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

At power-on, the FPGA attempts to configure itself automatically in SPI master mode, depending on the header of the bitstream that has been flashed into the card. This normally results in SPIx4 configuration at EMCCLK frequency. The configuration scheme used in the ADM-VPX3-9V2 is compatible with Multiboot; see Xilinx UG570 for details. The FPGA can also be made to reconfigure itself from an arbitrary Flash address using the ICAPE3 primitive; this is also described in Xilinx UG570.

The image loaded can also support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.10.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 256
- -interface SPIx4
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)

Program with vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu02g-spi-x1_x2_x4_x8
- State of non-config mem I/O pins: Pull-none

3.10.2 Configuration via JTAG

A Xilinx programming cable (HW-USB-II-G) can connect directly to the header on the debug board. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager. The device will be automatically recognized in Vivado Hardware Manager.

When the HW-USB-II-G is not plugged into the debug board, the JTAG channel is routed to the P0 standard JTAG connection.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug908-vivado-programming-debugging.pdf

3.11 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

Appendix A: Complete Pinout Table

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AY22	AUXCLK_DIR_1V8	IO_L11P_T1U_N8_GC_64	IO_L11P_T1U_N8_GC_64		1.8 (LVCMOS18)
AV24	AUXCLK_SE_1V8	IO_L14P_T2L_N2_GC_64	IO_L14P_T2L_N2_GC_64	P0.B8 - P0.C8	1.8 (LVCMOS18)
BC7	AVR_B2U_1V8	IO_L9N_T1L_N5_AD12N_68	IO_L9N_T1L_N5_AD12N_68		1.8 (LVCMOS18)
BA9	AVR_MON_CLK_1V8	IO_L12P_T1U_N10_GC_68	IO_L12P_T1U_N10_GC_68		1.8 (LVCMOS18)
BA7	AVR_U2B_1V8	IO_L10P_T1U_N6_QBC-_AD4P_68	IO_L10P_T1U_N6_QBC-_AD4P_68		1.8 (LVCMOS18)
AU22	AX_RESET_L	IO_L15P_T2L_N4_AD11P_64	IO_L15P_T2L_N4_AD11P_64	P1.G13	1.8 (LVCMOS18)
AG13	CCLK	CCLK_0	CCLK_0		1.2 (LVCMOS12)
AP29	DDR4_0_A0	IO_L21N_T3L_N5_AD8N_40	IO_L21N_T3L_N5_AD8N_61		1.2
BA29	DDR4_0_A1	IO_L9P_T1L_N4_AD12P_40	IO_L9P_T1L_N4_AD12P_61		1.2
AP30	DDR4_0_A10	IO_L20P_T3L_N2_AD1P_40	IO_L20P_T3L_N2_AD1P_61		1.2
AY32	DDR4_0_A11	IO_L12N_T1U_N11_GC_40	IO_L12N_T1U_N11_GC_61		1.2
BB31	DDR4_0_A12	IO_L8N_T1L_N3_AD5N_40	IO_L8N_T1L_N3_AD5N_61		1.2
AW31	DDR4_0_A13	IO_L14N_T2L_N3_GC_40	IO_L14N_T2L_N3_GC_61		1.2
AR31	DDR4_0_A14	IO_L19N_T3L_N1_DBC-_AD9N_40	IO_L19N_T3L_N1_DBC-_AD9N_61		1.2
AR30	DDR4_0_A15	IO_L20N_T3L_N3_AD1N_40	IO_L20N_T3L_N3_AD1N_61		1.2
AT29	DDR4_0_A2	IO_L18P_T2U_N10_AD-2P_40	IO_L18P_T2U_N10_AD-2P_61		1.2
AT30	DDR4_0_A3	IO_L18N_T2U_N11_AD-2N_40	IO_L18N_T2U_N11_AD-2N_61		1.2
AN29	DDR4_0_A4	IO_L21P_T3L_N4_AD8P_40	IO_L21P_T3L_N4_AD8P_61		1.2
AU32	DDR4_0_A5	IO_L15P_T2L_N4_AD11P_40	IO_L15P_T2L_N4_AD11P_61		1.2
AU31	DDR4_0_A6	IO_L17N_T2U_N9_AD1-0N_40	IO_L17N_T2U_N9_AD1-0N_61		1.2
AV31	DDR4_0_A7	IO_L14P_T2L_N2_GC_40	IO_L14P_T2L_N2_GC_61		1.2
AU30	DDR4_0_A8	IO_L17P_T2U_N8_AD1-0P_40	IO_L17P_T2U_N8_AD1-0P_61		1.2
BB29	DDR4_0_A9	IO_L9N_T1L_N5_AD12N_40	IO_L9N_T1L_N5_AD12N_61		1.2
AT32	DDR4_0_ACT_N	IO_T2U_N12_40	IO_T2U_N12_61		1.2
AV29	DDR4_0_ALERT_N	IO_L16N_T2U_N7_QBC-_AD3N_40	IO_L16N_T2U_N7_QBC-_AD3N_61		1.2
BA30	DDR4_0_BA0	IO_L11N_T1U_N9_GC_40	IO_L11N_T1U_N9_GC_61		1.2
BC33	DDR4_0_BA1	IO_T1U_N12_40	IO_T1U_N12_61		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AV32	DDR4_0_BG0	IO_L15N_T2L_N5_AD11N_40	IO_L15N_T2L_N5_AD11N_61		1.2
AP31	DDR4_0_CKE	IO_L19P_T3L_N0_DBC_AD9P_40	IO_L19P_T3L_N0_DBC_AD9P_61		1.2
BC32	DDR4_0_CLK_C	IO_L7N_T1L_N1_QBC_AD13N_40	IO_L7N_T1L_N1_QBC_AD13N_61		1.2
BC31	DDR4_0_CLK_T	IO_L7P_T1L_N0_QBC_AD13P_40	IO_L7P_T1L_N0_QBC_AD13P_61		1.2
BA32	DDR4_0_CS_0_N	IO_L10P_T1U_N6_QBC_AD4P_40	IO_L10P_T1U_N6_QBC_AD4P_61		1.2
AY31	DDR4_0_CS_1_N	IO_L12P_T1U_N10_GC_40	IO_L12P_T1U_N10_GC_61		1.2
BF32	DDR4_0_DM0	IO_L1P_T0L_N0_DBC_40	IO_L1P_T0L_N0_DBC_61		1.2
AT33	DDR4_0_DM1	IO_L19P_T3L_N0_DBC_AD9P_41	IO_L19P_T3L_N0_DBC_AD9P_62		1.2
BF39	DDR4_0_DM2	IO_L1P_T0L_N0_DBC_41	IO_L1P_T0L_N0_DBC_62		1.2
BA34	DDR4_0_DM3	IO_L13P_T2L_N0_GC_QBC_41	IO_L13P_T2L_N0_GC_QBC_62		1.2
BC34	DDR4_0_DM4	IO_L7P_T1L_N0_QBC_AD13P_41	IO_L7P_T1L_N0_QBC_AD13P_62		1.2
AA32	DDR4_0_DM5	IO_L19P_T3L_N0_DBC_AD9P_42	IO_L19P_T3L_N0_DBC_AD9P_63		1.2
AE31	DDR4_0_DM6	IO_L13P_T2L_N0_GC_QBC_42	IO_L13P_T2L_N0_GC_QBC_63		1.2
AH34	DDR4_0_DM7	IO_L7P_T1L_N0_QBC_AD13P_42	IO_L7P_T1L_N0_QBC_AD13P_63		1.2
AJ27	DDR4_0_DM8	IO_L1P_T0L_N0_DBC_42	IO_L1P_T0L_N0_DBC_63		1.2
BC29	DDR4_0_DQ0	IO_L6P_T0U_N10_AD6P_40	IO_L6P_T0U_N10_AD6P_61		1.2
BE30	DDR4_0_DQ1	IO_L3P_T0L_N4_AD15P_40	IO_L3P_T0L_N4_AD15P_61		1.2
AR33	DDR4_0_DQ10	IO_L20N_T3L_N3_AD1N_41	IO_L20N_T3L_N3_AD1N_62		1.2
AP34	DDR4_0_DQ11	IO_L21N_T3L_N5_AD8N_41	IO_L21N_T3L_N5_AD8N_62		1.2
AL32	DDR4_0_DQ12	IO_L23P_T3U_N8_41	IO_L23P_T3U_N8_62		1.2
AM34	DDR4_0_DQ13	IO_L24N_T3U_N11_41	IO_L24N_T3U_N11_62		1.2
AM32	DDR4_0_DQ14	IO_L23N_T3U_N9_41	IO_L23N_T3U_N9_62		1.2
AL34	DDR4_0_DQ15	IO_L24P_T3U_N10_41	IO_L24P_T3U_N10_62		1.2
BD39	DDR4_0_DQ16	IO_L5N_T0U_N9_AD14N_41	IO_L5N_T0U_N9_AD14N_62		1.2
BE37	DDR4_0_DQ17	IO_L3P_T0L_N4_AD15P_41	IO_L3P_T0L_N4_AD15P_62		1.2
BC39	DDR4_0_DQ18	IO_L5P_T0U_N8_AD14P_41	IO_L5P_T0U_N8_AD14P_62		1.2
BF38	DDR4_0_DQ19	IO_L2N_T0L_N3_41	IO_L2N_T0L_N3_62		1.2
BD29	DDR4_0_DQ2	IO_L6N_T0U_N11_AD6N_40	IO_L6N_T0U_N11_AD6N_61		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
BC38	DDR4_0_DQ20	IO_L6N_T0U_N11_AD6N_41	IO_L6N_T0U_N11_AD6N_62		1.2
BF37	DDR4_0_DQ21	IO_L3N_T0L_N5_AD15N_41	IO_L3N_T0L_N5_AD15N_62		1.2
BB38	DDR4_0_DQ22	IO_L6P_T0U_N10_AD6P_41	IO_L6P_T0U_N10_AD6P_62		1.2
BE38	DDR4_0_DQ23	IO_L2P_T0L_N2_41	IO_L2P_T0L_N2_62		1.2
AV33	DDR4_0_DQ24	IO_L18P_T2U_N10_AD2P_41	IO_L18P_T2U_N10_AD2P_62		1.2
AY36	DDR4_0_DQ25	IO_L14N_T2L_N3_GC_41	IO_L14N_T2L_N3_GC_62		1.2
AW33	DDR4_0_DQ26	IO_L18N_T2U_N11_AD2N_41	IO_L18N_T2U_N11_AD2N_62		1.2
AW34	DDR4_0_DQ27	IO_L17N_T2U_N9_AD10N_41	IO_L17N_T2U_N9_AD10N_62		1.2
BA33	DDR4_0_DQ28	IO_L15N_T2L_N5_AD11N_41	IO_L15N_T2L_N5_AD11N_62		1.2
AY35	DDR4_0_DQ29	IO_L14P_T2L_N2_GC_41	IO_L14P_T2L_N2_GC_62		1.2
BE31	DDR4_0_DQ3	IO_L2P_T0L_N2_40	IO_L2P_T0L_N2_61		1.2
AV34	DDR4_0_DQ30	IO_L17P_T2U_N8_AD10P_41	IO_L17P_T2U_N8_AD10P_62		1.2
AY33	DDR4_0_DQ31	IO_L15P_T2L_N4_AD11P_41	IO_L15P_T2L_N4_AD11P_62		1.2
BD36	DDR4_0_DQ32	IO_L9P_T1L_N4_AD12P_41	IO_L9P_T1L_N4_AD12P_62		1.2
BC36	DDR4_0_DQ33	IO_L11N_T1U_N9_GC_41	IO_L11N_T1U_N9_GC_62		1.2
BE36	DDR4_0_DQ34	IO_L9N_T1L_N5_AD12N_41	IO_L9N_T1L_N5_AD12N_62		1.2
BB36	DDR4_0_DQ35	IO_L11P_T1U_N8_GC_41	IO_L11P_T1U_N8_GC_62		1.2
BE35	DDR4_0_DQ36	IO_L8N_T1L_N3_AD5N_41	IO_L8N_T1L_N3_AD5N_62		1.2
BB35	DDR4_0_DQ37	IO_L12N_T1U_N11_GC_41	IO_L12N_T1U_N11_GC_62		1.2
BD35	DDR4_0_DQ38	IO_L8P_T1L_N2_AD5P_41	IO_L8P_T1L_N2_AD5P_62		1.2
BA35	DDR4_0_DQ39	IO_L12P_T1U_N10_GC_41	IO_L12P_T1U_N10_GC_62		1.2
BD33	DDR4_0_DQ4	IO_L5P_T0U_N8_AD14P_40	IO_L5P_T0U_N8_AD14P_61		1.2
AB34	DDR4_0_DQ40	IO_L20N_T3L_N3_AD1N_42	IO_L20N_T3L_N3_AD1N_63		1.2
Y33	DDR4_0_DQ41	IO_L23N_T3U_N9_42	IO_L23N_T3U_N9_63		1.2
AA34	DDR4_0_DQ42	IO_L20P_T3L_N2_AD1P_42	IO_L20P_T3L_N2_AD1P_63		1.2
W34	DDR4_0_DQ43	IO_L24N_T3U_N11_42	IO_L24N_T3U_N11_63		1.2
W30	DDR4_0_DQ44	IO_L21P_T3L_N4_AD8P_42	IO_L21P_T3L_N4_AD8P_63		1.2
W33	DDR4_0_DQ45	IO_L24P_T3U_N10_42	IO_L24P_T3U_N10_63		1.2
Y30	DDR4_0_DQ46	IO_L21N_T3L_N5_AD8N_42	IO_L21N_T3L_N5_AD8N_63		1.2
Y32	DDR4_0_DQ47	IO_L23P_T3U_N8_42	IO_L23P_T3U_N8_63		1.2
AD34	DDR4_0_DQ48	IO_L18N_T2U_N11_AD2N_42	IO_L18N_T2U_N11_AD2N_63		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AE33	DDR4_0_DQ49	IO_L14N_T2L_N3_GC_42	IO_L14N_T2L_N3_GC_63		1.2
BF30	DDR4_0_DQ5	IO_L3N_T0L_N5_AD15N_40	IO_L3N_T0L_N5_AD15N_61		1.2
AC34	DDR4_0_DQ50	IO_L18P_T2U_N10_AD-2P_42	IO_L18P_T2U_N10_AD-2P_63		1.2
AD33	DDR4_0_DQ51	IO_L14P_T2L_N2_GC_42	IO_L14P_T2L_N2_GC_63		1.2
AC33	DDR4_0_DQ52	IO_L17N_T2U_N9_AD1-0N_42	IO_L17N_T2U_N9_AD1-0N_63		1.2
AE30	DDR4_0_DQ53	IO_L15P_T2L_N4_AD11P_42	IO_L15P_T2L_N4_AD11P_63		1.2
AC32	DDR4_0_DQ54	IO_L17P_T2U_N8_AD1-0P_42	IO_L17P_T2U_N8_AD1-0P_63		1.2
AF30	DDR4_0_DQ55	IO_L15N_T2L_N5_AD11N_42	IO_L15N_T2L_N5_AD11N_63		1.2
AF33	DDR4_0_DQ56	IO_L12N_T1U_N11_GC_42	IO_L12N_T1U_N11_GC_63		1.2
AH33	DDR4_0_DQ57	IO_L8P_T1L_N2_AD5P_42	IO_L8P_T1L_N2_AD5P_63		1.2
AF34	DDR4_0_DQ58	IO_L9P_T1L_N4_AD12P_42	IO_L9P_T1L_N4_AD12P_63		1.2
AG34	DDR4_0_DQ59	IO_L9N_T1L_N5_AD12N_42	IO_L9N_T1L_N5_AD12N_63		1.2
BE33	DDR4_0_DQ6	IO_L5N_T0U_N9_AD14N_40	IO_L5N_T0U_N9_AD14N_61		1.2
AG31	DDR4_0_DQ60	IO_L11P_T1U_N8_GC_42	IO_L11P_T1U_N8_GC_63		1.2
AJ33	DDR4_0_DQ61	IO_L8N_T1L_N3_AD5N_42	IO_L8N_T1L_N3_AD5N_63		1.2
AF32	DDR4_0_DQ62	IO_L12P_T1U_N10_GC_42	IO_L12P_T1U_N10_GC_63		1.2
AG32	DDR4_0_DQ63	IO_L11N_T1U_N9_GC_42	IO_L11N_T1U_N9_GC_63		1.2
AK28	DDR4_0_DQ64	IO_L2N_T0L_N3_42	IO_L2N_T0L_N3_63		1.2
AK31	DDR4_0_DQ65	IO_L6N_T0U_N11_AD6N_42	IO_L6N_T0U_N11_AD6N_63		1.2
AJ30	DDR4_0_DQ66	IO_L3N_T0L_N5_AD15N_42	IO_L3N_T0L_N5_AD15N_63		1.2
AJ31	DDR4_0_DQ67	IO_L6P_T0U_N10_AD6P_42	IO_L6P_T0U_N10_AD6P_63		1.2
AJ28	DDR4_0_DQ68	IO_L2P_T0L_N2_42	IO_L2P_T0L_N2_63		1.2
AG30	DDR4_0_DQ69	IO_L5N_T0U_N9_AD14N_42	IO_L5N_T0U_N9_AD14N_63		1.2
BE32	DDR4_0_DQ7	IO_L2N_T0L_N3_40	IO_L2N_T0L_N3_61		1.2
AJ29	DDR4_0_DQ70	IO_L3P_T0L_N4_AD15P_42	IO_L3P_T0L_N4_AD15P_63		1.2
AG29	DDR4_0_DQ71	IO_L5P_T0U_N8_AD14P_42	IO_L5P_T0U_N8_AD14P_63		1.2
AP33	DDR4_0_DQ8	IO_L20P_T3L_N2_AD1P_41	IO_L20P_T3L_N2_AD1P_62		1.2
AN34	DDR4_0_DQ9	IO_L21P_T3L_N4_AD8P_41	IO_L21P_T3L_N4_AD8P_62		1.2
BD31	DDR4_0_DQS0_C	IO_L4N_T0U_N7_DBC_-AD7N_40	IO_L4N_T0U_N7_DBC_-AD7N_61		1.2
BD30	DDR4_0_DQS0_T	IO_L4P_T0U_N6_DBC_-AD7P_40	IO_L4P_T0U_N6_DBC_-AD7P_61		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AN33	DDR4_0_DQS1_C	IO_L22N_T3U_N7_DBC_AD0N_41	IO_L22N_T3U_N7_DBC_AD0N_62		1.2
AN32	DDR4_0_DQS1_T	IO_L22P_T3U_N6_DBC_AD0P_41	IO_L22P_T3U_N6_DBC_AD0P_62		1.2
BE40	DDR4_0_DQS2_C	IO_L4N_T0U_N7_DBC_AD7N_41	IO_L4N_T0U_N7_DBC_AD7N_62		1.2
BD40	DDR4_0_DQS2_T	IO_L4P_T0U_N6_DBC_AD7P_41	IO_L4P_T0U_N6_DBC_AD7P_62		1.2
AW36	DDR4_0_DQS3_C	IO_L16N_T2U_N7_QBC_AD3N_41	IO_L16N_T2U_N7_QBC_AD3N_62		1.2
AW35	DDR4_0_DQS3_T	IO_L16P_T2U_N6_QBC_AD3P_41	IO_L16P_T2U_N6_QBC_AD3P_62		1.2
BC37	DDR4_0_DQS4_C	IO_L10N_T1U_N7_QBC_AD4N_41	IO_L10N_T1U_N7_QBC_AD4N_62		1.2
BB37	DDR4_0_DQS4_T	IO_L10P_T1U_N6_QBC_AD4P_41	IO_L10P_T1U_N6_QBC_AD4P_62		1.2
Y31	DDR4_0_DQS5_C	IO_L22N_T3U_N7_DBC_AD0N_42	IO_L22N_T3U_N7_DBC_AD0N_63		1.2
W31	DDR4_0_DQS5_T	IO_L22P_T3U_N6_DBC_AD0P_42	IO_L22P_T3U_N6_DBC_AD0P_63		1.2
AD31	DDR4_0_DQS6_C	IO_L16N_T2U_N7_QBC_AD3N_42	IO_L16N_T2U_N7_QBC_AD3N_63		1.2
AC31	DDR4_0_DQS6_T	IO_L16P_T2U_N6_QBC_AD3P_42	IO_L16P_T2U_N6_QBC_AD3P_63		1.2
AH32	DDR4_0_DQS7_C	IO_L10N_T1U_N7_QBC_AD4N_42	IO_L10N_T1U_N7_QBC_AD4N_63		1.2
AH31	DDR4_0_DQS7_T	IO_L10P_T1U_N6_QBC_AD4P_42	IO_L10P_T1U_N6_QBC_AD4P_63		1.2
AH29	DDR4_0_DQS8_C	IO_L4N_T0U_N7_DBC_AD7N_42	IO_L4N_T0U_N7_DBC_AD7N_63		1.2
AH28	DDR4_0_DQS8_T	IO_L4P_T0U_N6_DBC_AD7P_42	IO_L4P_T0U_N6_DBC_AD7P_63		1.2
AM29	DDR4_0_ODT	IO_L22P_T3U_N6_DBC_AD0P_40	IO_L22P_T3U_N6_DBC_AD0P_61		1.2
BB30	DDR4_0_PARITY	IO_L8P_T1L_N2_AD5P_40	IO_L8P_T1L_N2_AD5P_61		1.2
AU29	DDR4_0_RAS_N	IO_L16P_T2U_N6_QBC_AD3P_40	IO_L16P_T2U_N6_QBC_AD3P_61		1.2
BB32	DDR4_0_RESET_N	IO_L10N_T1U_N7_QBC_AD4N_40	IO_L10N_T1U_N7_QBC_AD4N_61		1.2
AY30	DDR4_0_TEN	IO_L11P_T1U_N8_GC_40	IO_L11P_T1U_N8_GC_61		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
BA27	DDR4_1_A0	IO_L9P_T1L_N4_AD12P_A14_D30_65	IO_L9P_T1L_N4_AD12P_A14_D30_65		1.2
BB27	DDR4_1_A1	IO_L8N_T1L_N3_AD5N_A17_65	IO_L8N_T1L_N3_AD5N_A17_65		1.2
AT25	DDR4_1_A10	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65		1.2
AV27	DDR4_1_A11	IO_L14P_T2L_N2_GC_A04_D20_65	IO_L14P_T2L_N2_GC_A04_D20_65		1.2
AR25	DDR4_1_A12	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65		1.2
AU26	DDR4_1_A13	IO_L15P_T2L_N4_AD11P_A02_D18_65	IO_L15P_T2L_N4_AD11P_A02_D18_65		1.2
AR27	DDR4_1_A14	IO_L17P_T2U_N8_AD10P_D14_65	IO_L17P_T2U_N8_AD10P_D14_65		1.2
AT27	DDR4_1_A15	IO_L17N_T2U_N9_AD10N_D15_65	IO_L17N_T2U_N9_AD10N_D15_65		1.2
BC28	DDR4_1_A2	IO_T1U_N12_SMBALERT_65	IO_T1U_N12_SMBALERT_65		1.2
AY25	DDR4_1_A3	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65		1.2
BB26	DDR4_1_A4	IO_L8P_T1L_N2_AD5P_A16_65	IO_L8P_T1L_N2_AD5P_A16_65		1.2
AY26	DDR4_1_A5	IO_L11P_T1U_N8_GC_A10_D26_65	IO_L11P_T1U_N8_GC_A10_D26_65		1.2
AY27	DDR4_1_A6	IO_L11N_T1U_N9_GC_A11_D27_65	IO_L11N_T1U_N9_GC_A11_D27_65		1.2
BA28	DDR4_1_A7	IO_L9N_T1L_N5_AD12N_A15_D31_65	IO_L9N_T1L_N5_AD12N_A15_D31_65		1.2
AW28	DDR4_1_A8	IO_L12P_T1U_N10_GC_A08_D24_65	IO_L12P_T1U_N10_GC_A08_D24_65		1.2
AY28	DDR4_1_A9	IO_L12N_T1U_N11_GC_A09_D25_65	IO_L12N_T1U_N11_GC_A09_D25_65		1.2
AU25	DDR4_1_ACT_N	IO_T2U_N12_CSI_ADV_B_65	IO_T2U_N12_CSI_ADV_B_65		1.2
AP26	DDR4_1_ALERT_N	IO_L19N_T3L_N1_DBC_AD9N_D11_65	IO_L19N_T3L_N1_DBC_AD9N_D11_65		1.2
AP25	DDR4_1_BA0	IO_L19P_T3L_N0_DBC_AD9P_D10_65	IO_L19P_T3L_N0_DBC_AD9P_D10_65		1.2
AV28	DDR4_1_BA1	IO_L14N_T2L_N3_GC_A05_D21_65	IO_L14N_T2L_N3_GC_A05_D21_65		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AW25	DDR4_1_BG0	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65		1.2
AL25	DDR4_1_CKE	IO_L21P_T3L_N4_AD8P_D06_65	IO_L21P_T3L_N4_AD8P_D06_65		1.2
BB25	DDR4_1_CLK_C	IO_L7N_T1L_N1_QBC_AD13N_A19_65	IO_L7N_T1L_N1_QBC_AD13N_A19_65		1.2
BA25	DDR4_1_CLK_T	IO_L7P_T1L_N0_QBC_AD13P_A18_65	IO_L7P_T1L_N0_QBC_AD13P_A18_65		1.2
AM25	DDR4_1_CS_0_N	IO_L21N_T3L_N5_AD8N_D07_65	IO_L21N_T3L_N5_AD8N_D07_65		1.2
AR28	DDR4_1_CS_1_N	IO_L18P_T2U_N10_AD2P_D12_65	IO_L18P_T2U_N10_AD2P_D12_65		1.2
BE17	DDR4_1_DM0	IO_L1P_T0L_N0_DBC_66	IO_L1P_T0L_N0_DBC_66		1.2
AY17	DDR4_1_DM1	IO_L7P_T1L_N0_QBC_AD13P_66	IO_L7P_T1L_N0_QBC_AD13P_66		1.2
BF28	DDR4_1_DM2	IO_L1P_T0L_N0_DBC_RS0_65	IO_L1P_T0L_N0_DBC_RS0_65		1.2
AN18	DDR4_1_DM3	IO_L19P_T3L_N0_DBC_AD9P_66	IO_L19P_T3L_N0_DBC_AD9P_66		1.2
BF14	DDR4_1_DM4	IO_L1P_T0L_N0_DBC_67	IO_L1P_T0L_N0_DBC_67		1.2
BA12	DDR4_1_DM5	IO_L7P_T1L_N0_QBC_AD13P_67	IO_L7P_T1L_N0_QBC_AD13P_67		1.2
AW14	DDR4_1_DM6	IO_L13P_T2L_N0_GC_QBC_67	IO_L13P_T2L_N0_GC_QBC_67		1.2
AR16	DDR4_1_DM7	IO_L19P_T3L_N0_DBC_AD9P_67	IO_L19P_T3L_N0_DBC_AD9P_67		1.2
AT19	DDR4_1_DM8	IO_L13P_T2L_N0_GC_QBC_66	IO_L13P_T2L_N0_GC_QBC_66		1.2
BC18	DDR4_1_DQ0	IO_L6N_T0U_N11_AD6N_66	IO_L6N_T0U_N11_AD6N_66		1.2
BF18	DDR4_1_DQ1	IO_L2N_T0L_N3_66	IO_L2N_T0L_N3_66		1.2
AW18	DDR4_1_DQ10	IO_L11N_T1U_N9_GC_66	IO_L11N_T1U_N9_GC_66		1.2
AY18	DDR4_1_DQ11	IO_L8P_T1L_N2_AD5P_66	IO_L8P_T1L_N2_AD5P_66		1.2
AV19	DDR4_1_DQ12	IO_L12P_T1U_N10_GC_66	IO_L12P_T1U_N10_GC_66		1.2
AY20	DDR4_1_DQ13	IO_L9N_T1L_N5_AD12N_66	IO_L9N_T1L_N5_AD12N_66		1.2
AV18	DDR4_1_DQ14	IO_L11P_T1U_N8_GC_66	IO_L11P_T1U_N8_GC_66		1.2
AW20	DDR4_1_DQ15	IO_L9P_T1L_N4_AD12P_66	IO_L9P_T1L_N4_AD12P_66		1.2
BF27	DDR4_1_DQ16	IO_L2N_T0L_N3_FWE_FCS2_B_65	IO_L2N_T0L_N3_FWE_FCS2_B_65		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
BF25	DDR4_1_DQ17	IO_L5N_T0U_N9_AD14N_A23_65	IO_L5N_T0U_N9_AD14N_A23_65		1.2
BD28	DDR4_1_DQ18	IO_L3P_T0L_N4_AD15P_A26_65	IO_L3P_T0L_N4_AD15P_A26_65		1.2
BE25	DDR4_1_DQ19	IO_L5P_T0U_N8_AD14P_A22_65	IO_L5P_T0U_N8_AD14P_A22_65		1.2
BB19	DDR4_1_DQ2	IO_L6P_T0U_N10_AD6P_66	IO_L6P_T0U_N10_AD6P_66		1.2
BE27	DDR4_1_DQ20	IO_L2P_T0L_N2_FOE_B_65	IO_L2P_T0L_N2_FOE_B_65		1.2
BC26	DDR4_1_DQ21	IO_L6P_T0U_N10_AD6P_A20_65	IO_L6P_T0U_N10_AD6P_A20_65		1.2
BE28	DDR4_1_DQ22	IO_L3N_T0L_N5_AD15N_A27_65	IO_L3N_T0L_N5_AD15N_A27_65		1.2
BC27	DDR4_1_DQ23	IO_L6N_T0U_N11_AD6N_A21_65	IO_L6N_T0U_N11_AD6N_A21_65		1.2
AM19	DDR4_1_DQ24	IO_L23N_T3U_N9_66	IO_L23N_T3U_N9_66		1.2
AM16	DDR4_1_DQ25	IO_L21P_T3L_N4_AD8P_66	IO_L21P_T3L_N4_AD8P_66		1.2
AL19	DDR4_1_DQ26	IO_L23P_T3U_N8_66	IO_L23P_T3U_N8_66		1.2
AN19	DDR4_1_DQ27	IO_L20P_T3L_N2_AD1P_66	IO_L20P_T3L_N2_AD1P_66		1.2
AM20	DDR4_1_DQ28	IO_L24N_T3U_N11_66	IO_L24N_T3U_N11_66		1.2
AN16	DDR4_1_DQ29	IO_L21N_T3L_N5_AD8N_66	IO_L21N_T3L_N5_AD8N_66		1.2
BD18	DDR4_1_DQ3	IO_L3P_T0L_N4_AD15P_66	IO_L3P_T0L_N4_AD15P_66		1.2
AL20	DDR4_1_DQ30	IO_L24P_T3U_N10_66	IO_L24P_T3U_N10_66		1.2
AP19	DDR4_1_DQ31	IO_L20N_T3L_N3_AD1N_66	IO_L20N_T3L_N3_AD1N_66		1.2
BC14	DDR4_1_DQ32	IO_L6P_T0U_N10_AD6P_67	IO_L6P_T0U_N10_AD6P_67		1.2
BF15	DDR4_1_DQ33	IO_L2N_T0L_N3_67	IO_L2N_T0L_N3_67		1.2
BD15	DDR4_1_DQ34	IO_L5P_T0U_N8_AD14P_67	IO_L5P_T0U_N8_AD14P_67		1.2
BE16	DDR4_1_DQ35	IO_L3N_T0L_N5_AD15N_67	IO_L3N_T0L_N5_AD15N_67		1.2
BD14	DDR4_1_DQ36	IO_L5N_T0U_N9_AD14N_67	IO_L5N_T0U_N9_AD14N_67		1.2
BD16	DDR4_1_DQ37	IO_L3P_T0L_N4_AD15P_67	IO_L3P_T0L_N4_AD15P_67		1.2
BC13	DDR4_1_DQ38	IO_L6N_T0U_N11_AD6N_67	IO_L6N_T0U_N11_AD6N_67		1.2
BE15	DDR4_1_DQ39	IO_L2P_T0L_N2_67	IO_L2P_T0L_N2_67		1.2
BB17	DDR4_1_DQ4	IO_L5P_T0U_N8_AD14P_66	IO_L5P_T0U_N8_AD14P_66		1.2
AY16	DDR4_1_DQ40	IO_L9P_T1L_N4_AD12P_67	IO_L9P_T1L_N4_AD12P_67		1.2
AY12	DDR4_1_DQ41	IO_L8P_T1L_N2_AD5P_67	IO_L8P_T1L_N2_AD5P_67		1.2
BA14	DDR4_1_DQ42	IO_L11N_T1U_N9_GC_67	IO_L11N_T1U_N9_GC_67		1.2
AY11	DDR4_1_DQ43	IO_L8N_T1L_N3_AD5N_67	IO_L8N_T1L_N3_AD5N_67		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
BA15	DDR4_1_DQ44	IO_L11P_T1U_N8_GC_67	IO_L11P_T1U_N8_GC_67		1.2
AY13	DDR4_1_DQ45	IO_L12P_T1U_N10_GC_67	IO_L12P_T1U_N10_GC_67		1.2
AY15	DDR4_1_DQ46	IO_L9N_T1L_N5_AD12N_67	IO_L9N_T1L_N5_AD12N_67		1.2
BA13	DDR4_1_DQ47	IO_L12N_T1U_N11_GC_67	IO_L12N_T1U_N11_GC_67		1.2
AV13	DDR4_1_DQ48	IO_L15N_T2L_N5_AD11N_67	IO_L15N_T2L_N5_AD11N_67		1.2
AU15	DDR4_1_DQ49	IO_L17N_T2U_N9_AD10N_67	IO_L17N_T2U_N9_AD10N_67		1.2
BF19	DDR4_1_DQ5	IO_L2P_T0L_N2_66	IO_L2P_T0L_N2_66		1.2
AU13	DDR4_1_DQ50	IO_L15P_T2L_N4_AD11P_67	IO_L15P_T2L_N4_AD11P_67		1.2
AT15	DDR4_1_DQ51	IO_L17P_T2U_N8_AD10P_67	IO_L17P_T2U_N8_AD10P_67		1.2
AW15	DDR4_1_DQ52	IO_L14N_T2L_N3_GC_67	IO_L14N_T2L_N3_GC_67		1.2
AU16	DDR4_1_DQ53	IO_L18P_T2U_N10_AD2P_67	IO_L18P_T2U_N10_AD2P_67		1.2
AW16	DDR4_1_DQ54	IO_L14P_T2L_N2_GC_67	IO_L14P_T2L_N2_GC_67		1.2
AV16	DDR4_1_DQ55	IO_L18N_T2U_N11_AD2N_67	IO_L18N_T2U_N11_AD2N_67		1.2
AP14	DDR4_1_DQ56	IO_L20N_T3L_N3_AD1N_67	IO_L20N_T3L_N3_AD1N_67		1.2
AL14	DDR4_1_DQ57	IO_L24P_T3U_N10_67	IO_L24P_T3U_N10_67		1.2
AN13	DDR4_1_DQ58	IO_L21N_T3L_N5_AD8N_67	IO_L21N_T3L_N5_AD8N_67		1.2
AM15	DDR4_1_DQ59	IO_L23N_T3U_N9_67	IO_L23N_T3U_N9_67		1.2
BC17	DDR4_1_DQ6	IO_L5N_T0U_N9_AD14N_66	IO_L5N_T0U_N9_AD14N_66		1.2
AP15	DDR4_1_DQ60	IO_L20P_T3L_N2_AD1P_67	IO_L20P_T3L_N2_AD1P_67		1.2
AM14	DDR4_1_DQ61	IO_L24N_T3U_N11_67	IO_L24N_T3U_N11_67		1.2
AN14	DDR4_1_DQ62	IO_L21P_T3L_N4_AD8P_67	IO_L21P_T3L_N4_AD8P_67		1.2
AL15	DDR4_1_DQ63	IO_L23P_T3U_N8_67	IO_L23P_T3U_N8_67		1.2
AR20	DDR4_1_DQ64	IO_L18N_T2U_N11_AD2N_66	IO_L18N_T2U_N11_AD2N_66		1.2
AU17	DDR4_1_DQ65	IO_L15N_T2L_N5_AD11N_66	IO_L15N_T2L_N5_AD11N_66		1.2
AP18	DDR4_1_DQ66	IO_L17P_T2U_N8_AD10P_66	IO_L17P_T2U_N8_AD10P_66		1.2
AT18	DDR4_1_DQ67	IO_L15P_T2L_N4_AD11P_66	IO_L15P_T2L_N4_AD11P_66		1.2
AP20	DDR4_1_DQ68	IO_L18P_T2U_N10_AD2P_66	IO_L18P_T2U_N10_AD2P_66		1.2
AU20	DDR4_1_DQ69	IO_L14N_T2L_N3_GC_66	IO_L14N_T2L_N3_GC_66		1.2
BE18	DDR4_1_DQ7	IO_L3N_T0L_N5_AD15N_66	IO_L3N_T0L_N5_AD15N_66		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AR18	DDR4_1_DQ70	IO_L17N_T2U_N9_AD10N_66	IO_L17N_T2U_N9_AD10N_66		1.2
AT20	DDR4_1_DQ71	IO_L14P_T2L_N2_GC_66	IO_L14P_T2L_N2_GC_66		1.2
AW19	DDR4_1_DQ8	IO_L12N_T1U_N11_GC_66	IO_L12N_T1U_N11_GC_66		1.2
BA18	DDR4_1_DQ9	IO_L8N_T1L_N3_AD5N_66	IO_L8N_T1L_N3_AD5N_66		1.2
BD19	DDR4_1_DQS0_C	IO_L4N_T0U_N7_DBC_AD7N_66	IO_L4N_T0U_N7_DBC_AD7N_66		1.2
BC19	DDR4_1_DQS0_T	IO_L4P_T0U_N6_DBC_AD7P_66	IO_L4P_T0U_N6_DBC_AD7P_66		1.2
AW21	DDR4_1_DQS1_C	IO_L10N_T1U_N7_QBC_AD4N_66	IO_L10N_T1U_N7_QBC_AD4N_66		1.2
AV21	DDR4_1_DQS1_T	IO_L10P_T1U_N6_QBC_AD4P_66	IO_L10P_T1U_N6_QBC_AD4P_66		1.2
BE26	DDR4_1_DQS2_C	IO_L4N_T0U_N7_DBC_AD7N_A25_65	IO_L4N_T0U_N7_DBC_AD7N_A25_65		1.2
BD26	DDR4_1_DQS2_T	IO_L4P_T0U_N6_DBC_AD7P_A24_65	IO_L4P_T0U_N6_DBC_AD7P_A24_65		1.2
AM17	DDR4_1_DQS3_C	IO_L22N_T3U_N7_DBC_AD0N_66	IO_L22N_T3U_N7_DBC_AD0N_66		1.2
AL17	DDR4_1_DQS3_T	IO_L22P_T3U_N6_DBC_AD0P_66	IO_L22P_T3U_N6_DBC_AD0P_66		1.2
BE13	DDR4_1_DQS4_C	IO_L4N_T0U_N7_DBC_AD7N_67	IO_L4N_T0U_N7_DBC_AD7N_67		1.2
BD13	DDR4_1_DQS4_T	IO_L4P_T0U_N6_DBC_AD7P_67	IO_L4P_T0U_N6_DBC_AD7P_67		1.2
BB14	DDR4_1_DQS5_C	IO_L10N_T1U_N7_QBC_AD4N_67	IO_L10N_T1U_N7_QBC_AD4N_67		1.2
BB15	DDR4_1_DQS5_T	IO_L10P_T1U_N6_QBC_AD4P_67	IO_L10P_T1U_N6_QBC_AD4P_67		1.2
AV14	DDR4_1_DQS6_C	IO_L16N_T2U_N7_QBC_AD3N_67	IO_L16N_T2U_N7_QBC_AD3N_67		1.2
AU14	DDR4_1_DQS6_T	IO_L16P_T2U_N6_QBC_AD3P_67	IO_L16P_T2U_N6_QBC_AD3P_67		1.2
AR13	DDR4_1_DQS7_C	IO_L22N_T3U_N7_DBC_AD0N_67	IO_L22N_T3U_N7_DBC_AD0N_67		1.2
AP13	DDR4_1_DQS7_T	IO_L22P_T3U_N6_DBC_AD0P_67	IO_L22P_T3U_N6_DBC_AD0P_67		1.2
AT17	DDR4_1_DQS8_C	IO_L16N_T2U_N7_QBC_AD3N_66	IO_L16N_T2U_N7_QBC_AD3N_66		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AR17	DDR4_1_DQS8_T	IO_L16P_T2U_N6_QBC_AD3P_66	IO_L16P_T2U_N6_QBC_AD3P_66		1.2
AT28	DDR4_1_ODT	IO_L18N_T2U_N11_AD2N_D13_65	IO_L18N_T2U_N11_AD2N_D13_65		1.2
AN28	DDR4_1_PARITY	IO_L20P_T3L_N2_AD1P_D08_65	IO_L20P_T3L_N2_AD1P_D08_65		1.2
AM26	DDR4_1_RAS_N	IO_L22P_T3U_N6_DBC_AD0P_D04_65	IO_L22P_T3U_N6_DBC_AD0P_D04_65		1.2
AP28	DDR4_1_RESET_N	IO_L20N_T3L_N3_AD1N_D09_65	IO_L20N_T3L_N3_AD1N_D09_65		1.2
AU27	DDR4_1_TEN	IO_L15N_T2L_N5_AD11N_A03_D19_65	IO_L15N_T2L_N5_AD11N_A03_D19_65		1.2
B27	DDR4_2_A0	IO_L19N_T3L_N1_DBC_AD9N_48	IO_L19N_T3L_N1_DBC_AD9N_71		1.2
D28	DDR4_2_A1	IO_L18N_T2U_N11_AD2N_48	IO_L18N_T2U_N11_AD2N_71		1.2
A29	DDR4_2_A10	IO_L23N_T3U_N9_48	IO_L23N_T3U_N9_71		1.2
B30	DDR4_2_A11	IO_L24P_T3U_N10_48	IO_L24P_T3U_N10_71		1.2
C29	DDR4_2_A12	IO_L20N_T3L_N3_AD1N_48	IO_L20N_T3L_N3_AD1N_71		1.2
A30	DDR4_2_A13	IO_L24N_T3U_N11_48	IO_L24N_T3U_N11_71		1.2
M27	DDR4_2_A14	IO_L9P_T1L_N4_AD12P_48	IO_L9P_T1L_N4_AD12P_71		1.2
L27	DDR4_2_A15	IO_L9N_T1L_N5_AD12N_48	IO_L9N_T1L_N5_AD12N_71		1.2
A27	DDR4_2_A2	IO_L22P_T3U_N6_DBC_AD0P_48	IO_L22P_T3U_N6_DBC_AD0P_71		1.2
L28	DDR4_2_A3	IO_L8P_T1L_N2_AD5P_48	IO_L8P_T1L_N2_AD5P_71		1.2
A28	DDR4_2_A4	IO_L22N_T3U_N7_DBC_AD0N_48	IO_L22N_T3U_N7_DBC_AD0N_71		1.2
K28	DDR4_2_A5	IO_L8N_T1L_N3_AD5N_48	IO_L8N_T1L_N3_AD5N_71		1.2
H29	DDR4_2_A6	IO_L15P_T2L_N4_AD11P_48	IO_L15P_T2L_N4_AD11P_71		1.2
D30	DDR4_2_A7	IO_L21N_T3L_N5_AD8N_48	IO_L21N_T3L_N5_AD8N_71		1.2
E30	DDR4_2_A8	IO_L21P_T3L_N4_AD8P_48	IO_L21P_T3L_N4_AD8P_71		1.2
K26	DDR4_2_A9	IO_L10P_T1U_N6_QBC_AD4P_48	IO_L10P_T1U_N6_QBC_AD4P_71		1.2
E27	DDR4_2_ACT_N	IO_L17N_T2U_N9_AD10N_48	IO_L17N_T2U_N9_AD10N_71		1.2
E28	DDR4_2_ALERT_N	IO_L18P_T2U_N10_AD2P_48	IO_L18P_T2U_N10_AD2P_71		1.2
K27	DDR4_2_BA0	IO_L10N_T1U_N7_QBC_AD4N_48	IO_L10N_T1U_N7_QBC_AD4N_71		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
G27	DDR4_2_BA1	IO_L14N_T2L_N3_GC_48	IO_L14N_T2L_N3_GC_71		1.2
C27	DDR4_2_BG0	IO_L19P_T3L_N0_DBC_AD9P_48	IO_L19P_T3L_N0_DBC_AD9P_71		1.2
C28	DDR4_2_CKE	IO_T3U_N12_48	IO_T3U_N12_71		1.2
L29	DDR4_2_CLK_C	IO_L7N_T1L_N1_QBC_AD13N_48	IO_L7N_T1L_N1_QBC_AD13N_71		1.2
M29	DDR4_2_CLK_T	IO_L7P_T1L_N0_QBC_AD13P_48	IO_L7P_T1L_N0_QBC_AD13P_71		1.2
D29	DDR4_2_CS_0_N	IO_L20P_T3L_N2_AD1P_48	IO_L20P_T3L_N2_AD1P_71		1.2
F29	DDR4_2_CS_1_N	IO_L16N_T2U_N7_QBC_AD3N_48	IO_L16N_T2U_N7_QBC_AD3N_71		1.2
H37	DDR4_2_DM0	IO_L1P_T0L_N0_DBC_47	IO_L1P_T0L_N0_DBC_70		1.2
R30	DDR4_2_DM1	IO_L7P_T1L_N0_QBC_AD13P_46	IO_L7P_T1L_N0_QBC_AD13P_69		1.2
C36	DDR4_2_DM2	IO_L13P_T2L_N0_GC_QBC_47	IO_L13P_T2L_N0_GC_QBC_70		1.2
B34	DDR4_2_DM3	IO_L19P_T3L_N0_DBC_AD9P_47	IO_L19P_T3L_N0_DBC_AD9P_70		1.2
G30	DDR4_2_DM4	IO_L19P_T3L_N0_DBC_AD9P_46	IO_L19P_T3L_N0_DBC_AD9P_69		1.2
E40	DDR4_2_DM5	IO_L7P_T1L_N0_QBC_AD13P_47	IO_L7P_T1L_N0_QBC_AD13P_70		1.2
M31	DDR4_2_DM6	IO_L13P_T2L_N0_GC_QBC_46	IO_L13P_T2L_N0_GC_QBC_69		1.2
U34	DDR4_2_DM7	IO_L1P_T0L_N0_DBC_46	IO_L1P_T0L_N0_DBC_69		1.2
T28	DDR4_2_DM8	IO_L1P_T0L_N0_DBC_48	IO_L1P_T0L_N0_DBC_71		1.2
J36	DDR4_2_DQ0	IO_L3N_T0L_N5_AD15N_47	IO_L3N_T0L_N5_AD15N_70		1.2
G37	DDR4_2_DQ1	IO_L2P_T0L_N2_47	IO_L2P_T0L_N2_70		1.2
N31	DDR4_2_DQ10	IO_L11N_T1U_N9_GC_46	IO_L11N_T1U_N9_GC_69		1.2
P34	DDR4_2_DQ11	IO_L9P_T1L_N4_AD12P_46	IO_L9P_T1L_N4_AD12P_69		1.2
P31	DDR4_2_DQ12	IO_L11P_T1U_N8_GC_46	IO_L11P_T1U_N8_GC_69		1.2
N34	DDR4_2_DQ13	IO_L9N_T1L_N5_AD12N_46	IO_L9N_T1L_N5_AD12N_69		1.2
R32	DDR4_2_DQ14	IO_L8N_T1L_N3_AD5N_46	IO_L8N_T1L_N3_AD5N_69		1.2
N32	DDR4_2_DQ15	IO_L12P_T1U_N10_GC_46	IO_L12P_T1U_N10_GC_69		1.2
A35	DDR4_2_DQ16	IO_L17N_T2U_N9_AD10N_47	IO_L17N_T2U_N9_AD10N_70		1.2
A37	DDR4_2_DQ17	IO_L15P_T2L_N4_AD11P_47	IO_L15P_T2L_N4_AD11P_70		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
E35	DDR4_2_DQ18	IO_L18P_T2U_N10_AD2P_47	IO_L18P_T2U_N10_AD2P_70		1.2
A38	DDR4_2_DQ19	IO_L15N_T2L_N5_AD11N_47	IO_L15N_T2L_N5_AD11N_70		1.2
H34	DDR4_2_DQ2	IO_L5P_T0U_N8_AD14P_47	IO_L5P_T0U_N8_AD14P_70		1.2
B35	DDR4_2_DQ20	IO_L17P_T2U_N8_AD10P_47	IO_L17P_T2U_N8_AD10P_70		1.2
D36	DDR4_2_DQ21	IO_L14N_T2L_N3_GC_47	IO_L14N_T2L_N3_GC_70		1.2
D35	DDR4_2_DQ22	IO_L18N_T2U_N11_AD2N_47	IO_L18N_T2U_N11_AD2N_70		1.2
E36	DDR4_2_DQ23	IO_L14P_T2L_N2_GC_47	IO_L14P_T2L_N2_GC_70		1.2
C31	DDR4_2_DQ24	IO_L24N_T3U_N11_47	IO_L24N_T3U_N11_70		1.2
D34	DDR4_2_DQ25	IO_L20P_T3L_N2_AD1P_47	IO_L20P_T3L_N2_AD1P_70		1.2
D31	DDR4_2_DQ26	IO_L24P_T3U_N10_47	IO_L24P_T3U_N10_70		1.2
C33	DDR4_2_DQ27	IO_L21N_T3L_N5_AD8N_47	IO_L21N_T3L_N5_AD8N_70		1.2
B32	DDR4_2_DQ28	IO_L23N_T3U_N9_47	IO_L23N_T3U_N9_70		1.2
D33	DDR4_2_DQ29	IO_L21P_T3L_N4_AD8P_47	IO_L21P_T3L_N4_AD8P_70		1.2
F37	DDR4_2_DQ3	IO_L2N_T0L_N3_47	IO_L2N_T0L_N3_70		1.2
C32	DDR4_2_DQ30	IO_L23P_T3U_N8_47	IO_L23P_T3U_N8_70		1.2
C34	DDR4_2_DQ31	IO_L20N_T3L_N3_AD1N_47	IO_L20N_T3L_N3_AD1N_70		1.2
F33	DDR4_2_DQ32	IO_L24P_T3U_N10_46	IO_L24P_T3U_N10_69		1.2
G31	DDR4_2_DQ33	IO_L20N_T3L_N3_AD1N_46	IO_L20N_T3L_N3_AD1N_69		1.2
H32	DDR4_2_DQ34	IO_L21P_T3L_N4_AD8P_46	IO_L21P_T3L_N4_AD8P_69		1.2
E33	DDR4_2_DQ35	IO_L24N_T3U_N11_46	IO_L24N_T3U_N11_69		1.2
G32	DDR4_2_DQ36	IO_L21N_T3L_N5_AD8N_46	IO_L21N_T3L_N5_AD8N_69		1.2
F32	DDR4_2_DQ37	IO_L23P_T3U_N8_46	IO_L23P_T3U_N8_69		1.2
H31	DDR4_2_DQ38	IO_L20P_T3L_N2_AD1P_46	IO_L20P_T3L_N2_AD1P_69		1.2
E32	DDR4_2_DQ39	IO_L23N_T3U_N9_46	IO_L23N_T3U_N9_69		1.2
J35	DDR4_2_DQ4	IO_L3P_T0L_N4_AD15P_47	IO_L3P_T0L_N4_AD15P_70		1.2
E39	DDR4_2_DQ40	IO_L8P_T1L_N2_AD5P_47	IO_L8P_T1L_N2_AD5P_70		1.2
A40	DDR4_2_DQ41	IO_L9N_T1L_N5_AD12N_47	IO_L9N_T1L_N5_AD12N_70		1.2
D39	DDR4_2_DQ42	IO_L8N_T1L_N3_AD5N_47	IO_L8N_T1L_N3_AD5N_70		1.2
B40	DDR4_2_DQ43	IO_L9P_T1L_N4_AD12P_47	IO_L9P_T1L_N4_AD12P_70		1.2
E38	DDR4_2_DQ44	IO_L11P_T1U_N8_GC_47	IO_L11P_T1U_N8_GC_70		1.2
C39	DDR4_2_DQ45	IO_L12N_T1U_N11_GC_47	IO_L12N_T1U_N11_GC_70		1.2
D38	DDR4_2_DQ46	IO_L11N_T1U_N9_GC_47	IO_L11N_T1U_N9_GC_70		1.2
C38	DDR4_2_DQ47	IO_L12P_T1U_N10_GC_47	IO_L12P_T1U_N10_GC_70		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
K32	DDR4_2_DQ48	IO_L14N_T2L_N3_GC_46	IO_L14N_T2L_N3_GC_69		1.2
L33	DDR4_2_DQ49	IO_L18P_T2U_N10_AD2P_46	IO_L18P_T2U_N10_AD2P_69		1.2
F35	DDR4_2_DQ5	IO_L6N_T0U_N11_AD6N_47	IO_L6N_T0U_N11_AD6N_70		1.2
K33	DDR4_2_DQ50	IO_L18N_T2U_N11_AD2N_46	IO_L18N_T2U_N11_AD2N_69		1.2
L32	DDR4_2_DQ51	IO_L14P_T2L_N2_GC_46	IO_L14P_T2L_N2_GC_69		1.2
K31	DDR4_2_DQ52	IO_L17P_T2U_N8_AD10P_46	IO_L17P_T2U_N8_AD10P_69		1.2
L30	DDR4_2_DQ53	IO_L15N_T2L_N5_AD11N_46	IO_L15N_T2L_N5_AD11N_69		1.2
J31	DDR4_2_DQ54	IO_L17N_T2U_N9_AD10N_46	IO_L17N_T2U_N9_AD10N_69		1.2
M30	DDR4_2_DQ55	IO_L15P_T2L_N4_AD11P_46	IO_L15P_T2L_N4_AD11P_69		1.2
T32	DDR4_2_DQ56	IO_L3N_T0L_N5_AD15N_46	IO_L3N_T0L_N5_AD15N_69		1.2
T30	DDR4_2_DQ57	IO_L6N_T0U_N11_AD6N_46	IO_L6N_T0U_N11_AD6N_69		1.2
U32	DDR4_2_DQ58	IO_L3P_T0L_N4_AD15P_46	IO_L3P_T0L_N4_AD15P_69		1.2
V31	DDR4_2_DQ59	IO_L5P_T0U_N8_AD14P_46	IO_L5P_T0U_N8_AD14P_69		1.2
G34	DDR4_2_DQ6	IO_L5N_T0U_N9_AD14N_47	IO_L5N_T0U_N9_AD14N_70		1.2
R33	DDR4_2_DQ60	IO_L2N_T0L_N3_46	IO_L2N_T0L_N3_69		1.2
U31	DDR4_2_DQ61	IO_L5N_T0U_N9_AD14N_46	IO_L5N_T0U_N9_AD14N_69		1.2
T33	DDR4_2_DQ62	IO_L2P_T0L_N2_46	IO_L2P_T0L_N2_69		1.2
U30	DDR4_2_DQ63	IO_L6P_T0U_N10_AD6P_46	IO_L6P_T0U_N10_AD6P_69		1.2
P26	DDR4_2_DQ64	IO_L6P_T0U_N10_AD6P_48	IO_L6P_T0U_N10_AD6P_71		1.2
T27	DDR4_2_DQ65	IO_L2P_T0L_N2_48	IO_L2P_T0L_N2_71		1.2
T26	DDR4_2_DQ66	IO_L3P_T0L_N4_AD15P_48	IO_L3P_T0L_N4_AD15P_71		1.2
R27	DDR4_2_DQ67	IO_L2N_T0L_N3_48	IO_L2N_T0L_N3_71		1.2
N26	DDR4_2_DQ68	IO_L6N_T0U_N11_AD6N_48	IO_L6N_T0U_N11_AD6N_71		1.2
N28	DDR4_2_DQ69	IO_L5N_T0U_N9_AD14N_48	IO_L5N_T0U_N9_AD14N_71		1.2
F34	DDR4_2_DQ7	IO_L6P_T0U_N10_AD6P_47	IO_L6P_T0U_N10_AD6P_70		1.2
R26	DDR4_2_DQ70	IO_L3N_T0L_N5_AD15N_48	IO_L3N_T0L_N5_AD15N_71		1.2
P28	DDR4_2_DQ71	IO_L5P_T0U_N8_AD14P_48	IO_L5P_T0U_N8_AD14P_71		1.2
R31	DDR4_2_DQ8	IO_L8P_T1L_N2_AD5P_46	IO_L8P_T1L_N2_AD5P_69		1.2
N33	DDR4_2_DQ9	IO_L12N_T1U_N11_GC_46	IO_L12N_T1U_N11_GC_69		1.2
G36	DDR4_2_DQS0_C	IO_L4N_T0U_N7_DBC_AD7N_47	IO_L4N_T0U_N7_DBC_AD7N_70		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
H36	DDR4_2_DQS0_T	IO_L4P_T0U_N6_DBC_AD7P_47	IO_L4P_T0U_N6_DBC_AD7P_70		1.2
L34	DDR4_2_DQS1_C	IO_L10N_T1U_N7_QBC_AD4N_46	IO_L10N_T1U_N7_QBC_AD4N_69		1.2
M34	DDR4_2_DQS1_T	IO_L10P_T1U_N6_QBC_AD4P_46	IO_L10P_T1U_N6_QBC_AD4P_69		1.2
B37	DDR4_2_DQS2_C	IO_L16N_T2U_N7_QBC_AD3N_47	IO_L16N_T2U_N7_QBC_AD3N_70		1.2
B36	DDR4_2_DQS2_T	IO_L16P_T2U_N6_QBC_AD3P_47	IO_L16P_T2U_N6_QBC_AD3P_70		1.2
A33	DDR4_2_DQS3_C	IO_L22N_T3U_N7_DBC_AD0N_47	IO_L22N_T3U_N7_DBC_AD0N_70		1.2
A32	DDR4_2_DQS3_T	IO_L22P_T3U_N6_DBC_AD0P_47	IO_L22P_T3U_N6_DBC_AD0P_70		1.2
H33	DDR4_2_DQS4_C	IO_L22N_T3U_N7_DBC_AD0N_46	IO_L22N_T3U_N7_DBC_AD0N_69		1.2
J33	DDR4_2_DQS4_T	IO_L22P_T3U_N6_DBC_AD0P_46	IO_L22P_T3U_N6_DBC_AD0P_69		1.2
A39	DDR4_2_DQS5_C	IO_L10N_T1U_N7_QBC_AD4N_47	IO_L10N_T1U_N7_QBC_AD4N_70		1.2
B39	DDR4_2_DQS5_T	IO_L10P_T1U_N6_QBC_AD4P_47	IO_L10P_T1U_N6_QBC_AD4P_70		1.2
J30	DDR4_2_DQS6_C	IO_L16N_T2U_N7_QBC_AD3N_46	IO_L16N_T2U_N7_QBC_AD3N_69		1.2
K30	DDR4_2_DQS6_T	IO_L16P_T2U_N6_QBC_AD3P_46	IO_L16P_T2U_N6_QBC_AD3P_69		1.2
V33	DDR4_2_DQS7_C	IO_L4N_T0U_N7_DBC_AD7N_46	IO_L4N_T0U_N7_DBC_AD7N_69		1.2
V32	DDR4_2_DQS7_T	IO_L4P_T0U_N6_DBC_AD7P_46	IO_L4P_T0U_N6_DBC_AD7P_69		1.2
N29	DDR4_2_DQS8_C	IO_L4N_T0U_N7_DBC_AD7N_48	IO_L4N_T0U_N7_DBC_AD7N_71		1.2
P29	DDR4_2_DQS8_T	IO_L4P_T0U_N6_DBC_AD7P_48	IO_L4P_T0U_N6_DBC_AD7P_71		1.2
B29	DDR4_2_ODT	IO_L23P_T3U_N8_48	IO_L23P_T3U_N8_71		1.2
E26	DDR4_2_PARITY	IO_T2U_N12_48	IO_T2U_N12_71		1.2
G29	DDR4_2_RAS_N	IO_L15N_T2L_N5_AD11N_48	IO_L15N_T2L_N5_AD11N_71		1.2
F27	DDR4_2_RESET_N	IO_L17P_T2U_N8_AD10P_48	IO_L17P_T2U_N8_AD10P_71		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
F28	DDR4_2_TEN	IO_L16P_T2U_N6_QBC_AD3P_48	IO_L16P_T2U_N6_QBC_AD3P_71		1.2
E23	DDR4_3_A0	IO_L16P_T2U_N6_QBC_AD3P_72	IO_L16P_T2U_N6_QBC_AD3P_74		1.2
D24	DDR4_3_A1	IO_L17P_T2U_N8_AD10P_72	IO_L17P_T2U_N8_AD10P_74		1.2
F22	DDR4_3_A10	IO_L15N_T2L_N5_AD11N_72	IO_L15N_T2L_N5_AD11N_74		1.2
K25	DDR4_3_A11	IO_L10P_T1U_N6_QBC_AD4P_72	IO_L10P_T1U_N6_QBC_AD4P_74		1.2
D25	DDR4_3_A12	IO_L18N_T2U_N11_AD2N_72	IO_L18N_T2U_N11_AD2N_74		1.2
L23	DDR4_3_A13	IO_L9P_T1L_N4_AD12P_72	IO_L9P_T1L_N4_AD12P_74		1.2
K22	DDR4_3_A14	IO_L8N_T1L_N3_AD5N_72	IO_L8N_T1L_N3_AD5N_74		1.2
L22	DDR4_3_A15	IO_L8P_T1L_N2_AD5P_72	IO_L8P_T1L_N2_AD5P_74		1.2
F24	DDR4_3_A2	IO_L14P_T2L_N2_GC_72	IO_L14P_T2L_N2_GC_74		1.2
J23	DDR4_3_A3	IO_L11P_T1U_N8_GC_72	IO_L11P_T1U_N8_GC_74		1.2
F23	DDR4_3_A4	IO_L14N_T2L_N3_GC_72	IO_L14N_T2L_N3_GC_74		1.2
H24	DDR4_3_A5	IO_L12N_T1U_N11_GC_72	IO_L12N_T1U_N11_GC_74		1.2
J24	DDR4_3_A6	IO_L12P_T1U_N10_GC_72	IO_L12P_T1U_N10_GC_74		1.2
K23	DDR4_3_A7	IO_L9N_T1L_N5_AD12N_72	IO_L9N_T1L_N5_AD12N_74		1.2
J25	DDR4_3_A8	IO_L10N_T1U_N7_QBC_AD4N_72	IO_L10N_T1U_N7_QBC_AD4N_74		1.2
E25	DDR4_3_A9	IO_L18P_T2U_N10_AD2P_72	IO_L18P_T2U_N10_AD2P_74		1.2
G22	DDR4_3_ACT_N	IO_L15P_T2L_N4_AD11P_72	IO_L15P_T2L_N4_AD11P_74		1.2
D23	DDR4_3_ALERT_N	IO_L17N_T2U_N9_AD10N_72	IO_L17N_T2U_N9_AD10N_74		1.2
C23	DDR4_3_BA0	IO_L20N_T3L_N3_AD1N_72	IO_L20N_T3L_N3_AD1N_74		1.2
B26	DDR4_3_BA1	IO_L21N_T3L_N5_AD8N_72	IO_L21N_T3L_N5_AD8N_74		1.2
E22	DDR4_3_BG0	IO_L16N_T2U_N7_QBC_AD3N_72	IO_L16N_T2U_N7_QBC_AD3N_74		1.2
H22	DDR4_3_CKE	IO_T1U_N12_72	IO_T1U_N12_74		1.2
L24	DDR4_3_CLK_C	IO_L7N_T1L_N1_QBC_AD13N_72	IO_L7N_T1L_N1_QBC_AD13N_74		1.2
L25	DDR4_3_CLK_T	IO_L7P_T1L_N0_QBC_AD13P_72	IO_L7P_T1L_N0_QBC_AD13P_74		1.2
C24	DDR4_3_CS_0_N	IO_L20P_T3L_N2_AD1P_72	IO_L20P_T3L_N2_AD1P_74		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
C22	DDR4_3_CS_1_N	IO_L19P_T3L_N0_DBC_AD9P_72	IO_L19P_T3L_N0_DBC_AD9P_74		1.2
D19	DDR4_3_DM0	IO_L19P_T3L_N0_DBC_AD9P_71	IO_L19P_T3L_N0_DBC_AD9P_73		1.2
L17	DDR4_3_DM1	IO_L7P_T1L_N0_QBC_AD13P_71	IO_L7P_T1L_N0_QBC_AD13P_73		1.2
G14	DDR4_3_DM2	IO_L13P_T2L_N0_GC_QBC_70	IO_L13P_T2L_N0_GC_QBC_72		1.2
D13	DDR4_3_DM3	IO_L19P_T3L_N0_DBC_AD9P_70	IO_L19P_T3L_N0_DBC_AD9P_72		1.2
H19	DDR4_3_DM4	IO_L13P_T2L_N0_GC_QBC_71	IO_L13P_T2L_N0_GC_QBC_73		1.2
L13	DDR4_3_DM5	IO_L7P_T1L_N0_QBC_AD13P_70	IO_L7P_T1L_N0_QBC_AD13P_72		1.2
N17	DDR4_3_DM6	IO_L1P_T0L_N0_DBC_71	IO_L1P_T0L_N0_DBC_73		1.2
R21	DDR4_3_DM7	IO_L1P_T0L_N0_DBC_72	IO_L1P_T0L_N0_DBC_74		1.2
P13	DDR4_3_DM8	IO_L1P_T0L_N0_DBC_70	IO_L1P_T0L_N0_DBC_72		1.2
B19	DDR4_3_DQ0	IO_L23P_T3U_N8_71	IO_L23P_T3U_N8_73		1.2
D21	DDR4_3_DQ1	IO_L20P_T3L_N2_AD1P_71	IO_L20P_T3L_N2_AD1P_73		1.2
J20	DDR4_3_DQ10	IO_L12P_T1U_N10_GC_71	IO_L12P_T1U_N10_GC_73		1.2
J19	DDR4_3_DQ11	IO_L12N_T1U_N11_GC_71	IO_L12N_T1U_N11_GC_73		1.2
L20	DDR4_3_DQ12	IO_L9P_T1L_N4_AD12P_71	IO_L9P_T1L_N4_AD12P_73		1.2
K18	DDR4_3_DQ13	IO_L11P_T1U_N8_GC_71	IO_L11P_T1U_N8_GC_73		1.2
L19	DDR4_3_DQ14	IO_L8P_T1L_N2_AD5P_71	IO_L8P_T1L_N2_AD5P_73		1.2
L18	DDR4_3_DQ15	IO_L8N_T1L_N3_AD5N_71	IO_L8N_T1L_N3_AD5N_73		1.2
E13	DDR4_3_DQ16	IO_L15N_T2L_N5_AD11N_70	IO_L15N_T2L_N5_AD11N_72		1.2
E15	DDR4_3_DQ17	IO_L17P_T2U_N8_AD10P_70	IO_L17P_T2U_N8_AD10P_72		1.2
F13	DDR4_3_DQ18	IO_L15P_T2L_N4_AD11P_70	IO_L15P_T2L_N4_AD11P_72		1.2
D15	DDR4_3_DQ19	IO_L17N_T2U_N9_AD10N_70	IO_L17N_T2U_N9_AD10N_72		1.2
A19	DDR4_3_DQ2	IO_L23N_T3U_N9_71	IO_L23N_T3U_N9_73		1.2
F15	DDR4_3_DQ20	IO_L14N_T2L_N3_GC_70	IO_L14N_T2L_N3_GC_72		1.2
D16	DDR4_3_DQ21	IO_L18N_T2U_N11_AD2N_70	IO_L18N_T2U_N11_AD2N_72		1.2
G15	DDR4_3_DQ22	IO_L14P_T2L_N2_GC_70	IO_L14P_T2L_N2_GC_72		1.2
E16	DDR4_3_DQ23	IO_L18P_T2U_N10_AD2P_70	IO_L18P_T2U_N10_AD2P_72		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
C14	DDR4_3_DQ24	IO_L20P_T3L_N2_AD1P_70	IO_L20P_T3L_N2_AD1P_72		1.2
A14	DDR4_3_DQ25	IO_L21P_T3L_N4_AD8P_70	IO_L21P_T3L_N4_AD8P_72		1.2
B14	DDR4_3_DQ26	IO_L20N_T3L_N3_AD1N_70	IO_L20N_T3L_N3_AD1N_72		1.2
A13	DDR4_3_DQ27	IO_L21N_T3L_N5_AD8N_70	IO_L21N_T3L_N5_AD8N_72		1.2
C16	DDR4_3_DQ28	IO_L23P_T3U_N8_70	IO_L23P_T3U_N8_72		1.2
B16	DDR4_3_DQ29	IO_L23N_T3U_N9_70	IO_L23N_T3U_N9_72		1.2
C21	DDR4_3_DQ3	IO_L21P_T3L_N4_AD8P_71	IO_L21P_T3L_N4_AD8P_73		1.2
B17	DDR4_3_DQ30	IO_L24P_T3U_N10_70	IO_L24P_T3U_N10_72		1.2
A17	DDR4_3_DQ31	IO_L24N_T3U_N11_70	IO_L24N_T3U_N11_72		1.2
F20	DDR4_3_DQ32	IO_L15P_T2L_N4_AD11P_71	IO_L15P_T2L_N4_AD11P_73		1.2
F17	DDR4_3_DQ33	IO_L18N_T2U_N11_AD2N_71	IO_L18N_T2U_N11_AD2N_73		1.2
E20	DDR4_3_DQ34	IO_L17N_T2U_N9_AD10N_71	IO_L17N_T2U_N9_AD10N_73		1.2
F18	DDR4_3_DQ35	IO_L18P_T2U_N10_AD2P_71	IO_L18P_T2U_N10_AD2P_73		1.2
E21	DDR4_3_DQ36	IO_L17P_T2U_N8_AD10P_71	IO_L17P_T2U_N8_AD10P_73		1.2
F19	DDR4_3_DQ37	IO_L15N_T2L_N5_AD11N_71	IO_L15N_T2L_N5_AD11N_73		1.2
G20	DDR4_3_DQ38	IO_L14P_T2L_N2_GC_71	IO_L14P_T2L_N2_GC_73		1.2
G19	DDR4_3_DQ39	IO_L14N_T2L_N3_GC_71	IO_L14N_T2L_N3_GC_73		1.2
B20	DDR4_3_DQ4	IO_L24P_T3U_N10_71	IO_L24P_T3U_N10_73		1.2
J14	DDR4_3_DQ40	IO_L11P_T1U_N8_GC_70	IO_L11P_T1U_N8_GC_72		1.2
K15	DDR4_3_DQ41	IO_L8N_T1L_N3_AD5N_70	IO_L8N_T1L_N3_AD5N_72		1.2
J13	DDR4_3_DQ42	IO_L9P_T1L_N4_AD12P_70	IO_L9P_T1L_N4_AD12P_72		1.2
J15	DDR4_3_DQ43	IO_L12N_T1U_N11_GC_70	IO_L12N_T1U_N11_GC_72		1.2
H14	DDR4_3_DQ44	IO_L11N_T1U_N9_GC_70	IO_L11N_T1U_N9_GC_72		1.2
J16	DDR4_3_DQ45	IO_L12P_T1U_N10_GC_70	IO_L12P_T1U_N10_GC_72		1.2
H13	DDR4_3_DQ46	IO_L9N_T1L_N5_AD12N_70	IO_L9N_T1L_N5_AD12N_72		1.2
K16	DDR4_3_DQ47	IO_L8P_T1L_N2_AD5P_70	IO_L8P_T1L_N2_AD5P_72		1.2
R20	DDR4_3_DQ48	IO_L5P_T0U_N8_AD14P_71	IO_L5P_T0U_N8_AD14P_73		1.2
N18	DDR4_3_DQ49	IO_L2N_T0L_N3_71	IO_L2N_T0L_N3_73		1.2
D20	DDR4_3_DQ5	IO_L20N_T3L_N3_AD1N_71	IO_L20N_T3L_N3_AD1N_73		1.2
N21	DDR4_3_DQ50	IO_L6P_T0U_N10_AD6P_71	IO_L6P_T0U_N10_AD6P_73		1.2
P18	DDR4_3_DQ51	IO_L2P_T0L_N2_71	IO_L2P_T0L_N2_73		1.2
P20	DDR4_3_DQ52	IO_L5N_T0U_N9_AD14N_71	IO_L5N_T0U_N9_AD14N_73		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
M19	DDR4_3_DQ53	IO_L3N_T0L_N5_AD15N_71	IO_L3N_T0L_N5_AD15N_73		1.2
M21	DDR4_3_DQ54	IO_L6N_T0U_N11_AD6N_71	IO_L6N_T0U_N11_AD6N_73		1.2
M20	DDR4_3_DQ55	IO_L3P_T0L_N4_AD15P_71	IO_L3P_T0L_N4_AD15P_73		1.2
M25	DDR4_3_DQ56	IO_L5P_T0U_N8_AD14P_72	IO_L5P_T0U_N8_AD14P_74		1.2
N22	DDR4_3_DQ57	IO_L2P_T0L_N2_72	IO_L2P_T0L_N2_74		1.2
P23	DDR4_3_DQ58	IO_L3P_T0L_N4_AD15P_72	IO_L3P_T0L_N4_AD15P_74		1.2
N23	DDR4_3_DQ59	IO_L3N_T0L_N5_AD15N_72	IO_L3N_T0L_N5_AD15N_74		1.2
A20	DDR4_3_DQ6	IO_L24N_T3U_N11_71	IO_L24N_T3U_N11_73		1.2
P25	DDR4_3_DQ60	IO_L6N_T0U_N11_AD6N_72	IO_L6N_T0U_N11_AD6N_74		1.2
M24	DDR4_3_DQ61	IO_L5N_T0U_N9_AD14N_72	IO_L5N_T0U_N9_AD14N_74		1.2
R25	DDR4_3_DQ62	IO_L6P_T0U_N10_AD6P_72	IO_L6P_T0U_N10_AD6P_74		1.2
M22	DDR4_3_DQ63	IO_L2N_T0L_N3_72	IO_L2N_T0L_N3_74		1.2
N16	DDR4_3_DQ64	IO_L6P_T0U_N10_AD6P_70	IO_L6P_T0U_N10_AD6P_72		1.2
N14	DDR4_3_DQ65	IO_L2N_T0L_N3_70	IO_L2N_T0L_N3_72		1.2
M14	DDR4_3_DQ66	IO_L5P_T0U_N8_AD14P_70	IO_L5P_T0U_N8_AD14P_72		1.2
P14	DDR4_3_DQ67	IO_L2P_T0L_N2_70	IO_L2P_T0L_N2_72		1.2
M16	DDR4_3_DQ68	IO_L6N_T0U_N11_AD6N_70	IO_L6N_T0U_N11_AD6N_72		1.2
P15	DDR4_3_DQ69	IO_L3N_T0L_N5_AD15N_70	IO_L3N_T0L_N5_AD15N_72		1.2
B21	DDR4_3_DQ7	IO_L21N_T3L_N5_AD8N_71	IO_L21N_T3L_N5_AD8N_73		1.2
L14	DDR4_3_DQ70	IO_L5N_T0U_N9_AD14N_70	IO_L5N_T0U_N9_AD14N_72		1.2
R15	DDR4_3_DQ71	IO_L3P_T0L_N4_AD15P_70	IO_L3P_T0L_N4_AD15P_72		1.2
K20	DDR4_3_DQ8	IO_L9N_T1L_N5_AD12N_71	IO_L9N_T1L_N5_AD12N_73		1.2
J18	DDR4_3_DQ9	IO_L11N_T1U_N9_GC_71	IO_L11N_T1U_N9_GC_73		1.2
C18	DDR4_3_DQS0_C	IO_L22N_T3U_N7_DBC-_AD0N_71	IO_L22N_T3U_N7_DBC-_AD0N_73		1.2
D18	DDR4_3_DQS0_T	IO_L22P_T3U_N6_DBC-_AD0P_71	IO_L22P_T3U_N6_DBC-_AD0P_73		1.2
H21	DDR4_3_DQS1_C	IO_L10N_T1U_N7_QBC-_AD4N_71	IO_L10N_T1U_N7_QBC-_AD4N_73		1.2
J21	DDR4_3_DQS1_T	IO_L10P_T1U_N6_QBC-_AD4P_71	IO_L10P_T1U_N6_QBC-_AD4P_73		1.2
G16	DDR4_3_DQS2_C	IO_L16N_T2U_N7_QBC-_AD3N_70	IO_L16N_T2U_N7_QBC-_AD3N_72		1.2
G17	DDR4_3_DQS2_T	IO_L16P_T2U_N6_QBC-_AD3P_70	IO_L16P_T2U_N6_QBC-_AD3P_72		1.2
A15	DDR4_3_DQS3_C	IO_L22N_T3U_N7_DBC-_AD0N_70	IO_L22N_T3U_N7_DBC-_AD0N_72		1.2

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
B15	DDR4_3_DQS3_T	IO_L22P_T3U_N6_DBC_AD0P_70	IO_L22P_T3U_N6_DBC_AD0P_72		1.2
E17	DDR4_3_DQS4_C	IO_L16N_T2U_N7_QBC_AD3N_71	IO_L16N_T2U_N7_QBC_AD3N_73		1.2
E18	DDR4_3_DQS4_T	IO_L16P_T2U_N6_QBC_AD3P_71	IO_L16P_T2U_N6_QBC_AD3P_73		1.2
H16	DDR4_3_DQS5_C	IO_L10N_T1U_N7_QBC_AD4N_70	IO_L10N_T1U_N7_QBC_AD4N_72		1.2
H17	DDR4_3_DQS5_T	IO_L10P_T1U_N6_QBC_AD4P_70	IO_L10P_T1U_N6_QBC_AD4P_72		1.2
N19	DDR4_3_DQS6_C	IO_L4N_T0U_N7_DBC_AD7N_71	IO_L4N_T0U_N7_DBC_AD7N_73		1.2
P19	DDR4_3_DQS6_T	IO_L4P_T0U_N6_DBC_AD7P_71	IO_L4P_T0U_N6_DBC_AD7P_73		1.2
N24	DDR4_3_DQS7_C	IO_L4N_T0U_N7_DBC_AD7N_72	IO_L4N_T0U_N7_DBC_AD7N_74		1.2
P24	DDR4_3_DQS7_T	IO_L4P_T0U_N6_DBC_AD7P_72	IO_L4P_T0U_N6_DBC_AD7P_74		1.2
P16	DDR4_3_DQS8_C	IO_L4N_T0U_N7_DBC_AD7N_70	IO_L4N_T0U_N7_DBC_AD7N_72		1.2
R16	DDR4_3_DQS8_T	IO_L4P_T0U_N6_DBC_AD7P_70	IO_L4P_T0U_N6_DBC_AD7P_72		1.2
H23	DDR4_3_ODT	IO_L11N_T1U_N9_GC_72	IO_L11N_T1U_N9_GC_74		1.2
F25	DDR4_3_PARITY	IO_T2U_N12_72	IO_T2U_N12_74		1.2
B22	DDR4_3_RAS_N	IO_L19N_T3L_N1_DBC_AD9N_72	IO_L19N_T3L_N1_DBC_AD9N_74		1.2
C26	DDR4_3_RESET_N	IO_L21P_T3L_N4_AD8P_72	IO_L21P_T3L_N4_AD8P_74		1.2
A23	DDR4_3_TEN	IO_L22P_T3U_N6_DBC_AD0P_72	IO_L22P_T3U_N6_DBC_AD0P_74		1.2
AC12	DONE_1V8	DONE_0	DONE_0		1.8 (STARTUPE3)
AJ18	DXN_N	DXN	DXN		NA
AJ19	DXP_P	DXP	DXP		NA
AL27	EMCCLK_PIN	IO_L24P_T3U_N10_EMCCLK_65	IO_L24P_T3U_N10_EMCCLK_65		1.2 (LVCMOS12)
AF1	ETH1_RX_PIN_N	MGTYRXN3_227	MGTYRXN3_227	P1.C16	MGT
AF2	ETH1_RX_PIN_P	MGTYRXP3_227	MGTYRXP3_227	P1.B16	MGT
AF6	ETH1_TX_PIN_N	MGTYTXN3_227	MGTYTXN3_227	P1.F16	MGT
AF7	ETH1_TX_PIN_P	MGTYTXP3_227	MGTYTXP3_227	P1.E16	MGT
AG3	ETH2_RX_PIN_N	MGTYRXN2_227	MGTYRXN2_227	P1.B15	MGT

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AG4	ETH2_RX_PIN_P	MGTYRXP2_227	MGTYRXP2_227	P1.A15	MGT
AG8	ETH2_TX_PIN_N	MGTYTXN2_227	MGTYTXN2_227	P1.E15	MGT
AG9	ETH2_TX_PIN_P	MGTYTXP2_227	MGTYTXP2_227	P1.D15	MGT
BA23	FABRIC_CLK_N	IO_L12N_T1U_N11_GC_64	IO_L12N_T1U_N11_GC_64		1.8 (LVDS with DIFF_TERM_ADV)
AY23	FABRIC_CLK_P	IO_L12P_T1U_N10_GC_64	IO_L12P_T1U_N10_GC_64		1.8 (LVDS with DIFF_TERM_ADV)
BF10	FIREFLY_0_INT_L	IO_L3P_T0L_N4_AD15P_68	IO_L3P_T0L_N4_AD15P_68	J8.5	1.8 (LVCMOS18)
BF8	FIREFLY_0_MODPRS_L	IO_L2N_T0L_N3_68	IO_L2N_T0L_N3_68	J8.3	1.8 (LVCMOS18)
BE7	FIREFLY_0_RST_1V8_L	IO_L1P_T0L_N0_DBC_68	IO_L1P_T0L_N0_DBC_68	J8.6	1.8 (LVCMOS18)
AE46	FIREFLY_0_RX0_N	MGTYRXN0_124	MGTYRXN0_128	J6.B18	MGT
AE45	FIREFLY_0_RX0_P	MGTYRXP0_124	MGTYRXP0_128	J6.B17	MGT
AD44	FIREFLY_0_RX1_N	MGTYRXN1_124	MGTYRXN1_128	J6.A18	MGT
AD43	FIREFLY_0_RX1_P	MGTYRXP1_124	MGTYRXP1_128	J6.A17	MGT
AC46	FIREFLY_0_RX2_N	MGTYRXN2_124	MGTYRXN2_128	J6.B15	MGT
AC45	FIREFLY_0_RX2_P	MGTYRXP2_124	MGTYRXP2_128	J6.B14	MGT
AB44	FIREFLY_0_RX3_N	MGTYRXN3_124	MGTYRXN3_128	J6.A15	MGT
AB43	FIREFLY_0_RX3_P	MGTYRXP3_124	MGTYRXP3_128	J6.A14	MGT
BE8	FIREFLY_0_SCL_1V8	IO_L2P_T0L_N2_68	IO_L2P_T0L_N2_68	J8.8	1.8 (LVCMOS18)
BF7	FIREFLY_0_SDA_1V8	IO_L1N_T0L_N1_DBC_68	IO_L1N_T0L_N1_DBC_68	J8.7	1.8 (LVCMOS18)
AE41	FIREFLY_0_TX0_N	MGTYTXN0_124	MGTYTXN0_128	J6.A2	MGT
AE40	FIREFLY_0_TX0_P	MGTYTXP0_124	MGTYTXP0_128	J6.A3	MGT
AD39	FIREFLY_0_TX1_N	MGTYTXN1_124	MGTYTXN1_128	J6.B2	MGT
AD38	FIREFLY_0_TX1_P	MGTYTXP1_124	MGTYTXP1_128	J6.B3	MGT
AC41	FIREFLY_0_TX2_N	MGTYTXN2_124	MGTYTXN2_128	J6.A5	MGT
AC40	FIREFLY_0_TX2_P	MGTYTXP2_124	MGTYTXP2_128	J6.A6	MGT
AB39	FIREFLY_0_TX3_N	MGTYTXN3_124	MGTYTXN3_128	J6.B5	MGT
AB38	FIREFLY_0_TX3_P	MGTYTXP3_124	MGTYTXP3_128	J6.B6	MGT
BE11	FIREFLY_1_INT_L	IO_L4P_T0U_N6_DBC_AD7P_68	IO_L4P_T0U_N6_DBC_AD7P_68	J14.5	1.8 (LVCMOS18)
BF9	FIREFLY_1_MODPRS_L	IO_L3N_T0L_N5_AD15N_68	IO_L3N_T0L_N5_AD15N_68	J14.3	1.8 (LVCMOS18)
BE10	FIREFLY_1_RST_1V8_L	IO_L4N_T0U_N7_DBC_AD7N_68	IO_L4N_T0U_N7_DBC_AD7N_68	J14.6	1.8 (LVCMOS18)

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AA46	FIREFLY_1_RX0_N	MGTYRXN0_125	MGTYRXN0_129	J15.B18	MGT
AA45	FIREFLY_1_RX0_P	MGTYRXP0_125	MGTYRXP0_129	J15.B17	MGT
Y44	FIREFLY_1_RX1_N	MGTYRXN1_125	MGTYRXN1_129	J15.A18	MGT
Y43	FIREFLY_1_RX1_P	MGTYRXP1_125	MGTYRXP1_129	J15.A17	MGT
W46	FIREFLY_1_RX2_N	MGTYRXN2_125	MGTYRXN2_129	J15.B15	MGT
W45	FIREFLY_1_RX2_P	MGTYRXP2_125	MGTYRXP2_129	J15.B14	MGT
V44	FIREFLY_1_RX3_N	MGTYRXN3_125	MGTYRXN3_129	J15.A15	MGT
V43	FIREFLY_1_RX3_P	MGTYRXP3_125	MGTYRXP3_129	J15.A14	MGT
BF12	FIREFLY_1_SCL_1V8	IO_L5N_T0U_N9_AD14N_68	IO_L5N_T0U_N9_AD14N_68	J14.8	1.8 (LVCMOS18)
BE12	FIREFLY_1_SDA_1V8	IO_L5P_T0U_N8_AD14P_68	IO_L5P_T0U_N8_AD14P_68	J14.7	1.8 (LVCMOS18)
AA41	FIREFLY_1_TX0_N	MGTYTXN0_125	MGTYTXN0_129	J15.A2	MGT
AA40	FIREFLY_1_TX0_P	MGTYTXP0_125	MGTYTXP0_129	J15.A3	MGT
Y39	FIREFLY_1_TX1_N	MGTYTXN1_125	MGTYTXN1_129	J15.B2	MGT
Y38	FIREFLY_1_TX1_P	MGTYTXP1_125	MGTYTXP1_129	J15.B3	MGT
W41	FIREFLY_1_TX2_N	MGTYTXN2_125	MGTYTXN2_129	J15.A5	MGT
W40	FIREFLY_1_TX2_P	MGTYTXP2_125	MGTYTXP2_129	J15.A6	MGT
V39	FIREFLY_1_TX3_N	MGTYTXN3_125	MGTYTXN3_129	J15.B5	MGT
V38	FIREFLY_1_TX3_P	MGTYTXP3_125	MGTYTXP3_129	J15.B6	MGT
AG12	FPGA_FLASH_CE_L	RDWR_FCS_B_0	RDWR_FCS_B_0		1.8 (STARTUPE3)
AK12	FPGA_FLASH_DQ0	D00_MOSI_0	D00_MOSI_0		1.8 (STARTUPE3)
AJ12	FPGA_FLASH_DQ1	D01_DIN_0	D01_DIN_0		1.8 (STARTUPE3)
AL12	FPGA_FLASH_DQ2	D02_0	D02_0		1.8 (STARTUPE3)
AH12	FPGA_FLASH_DQ3	D03_0	D03_0		1.8 (STARTUPE3)
AT23	FPGA_GA0	IO_L17N_T2U_N9_AD10N_64	IO_L17N_T2U_N9_AD10N_64	P0.A6	1.8 (LVCMOS18)
AT24	FPGA_GA1	IO_L18P_T2U_N10_AD2P_64	IO_L18P_T2U_N10_AD2P_64	P0.B6	1.8 (LVCMOS18)
AU24	FPGA_GA2	IO_L18N_T2U_N11_AD2N_64	IO_L18N_T2U_N11_AD2N_64	P0.F6	1.8 (LVCMOS18)
AR21	FPGA_GA3	IO_T2U_N12_64	IO_T2U_N12_64	P0.G6	1.8 (LVCMOS18)
AN22	FPGA_GA4	IO_L19P_T3L_N0_DBC_AD9P_64	IO_L19P_T3L_N0_DBC_AD9P_64	P0.F5	1.8 (LVCMOS18)
AN21	FPGA_GAP	IO_L19N_T3L_N1_DBC_AD9N_64	IO_L19N_T3L_N1_DBC_AD9N_64	P0.G5	1.8 (LVCMOS18)
BB7	FPGA_I2C_EN	IO_L10N_T1U_N7_QBC_AD4N_68	IO_L10N_T1U_N7_QBC_AD4N_68		1.8 (LVCMOS18)

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AM27	FPGA_SCLK_1V8	IO_L23P_T3U_N8_I2C_SCLK_65	IO_L23P_T3U_N8_I2C_SCLK_65		1.8 (LVCMOS18)
AN27	FPGA_SDA_1V8	IO_L23N_T3U_N9_PERSTN1_I2C_SDA_65	IO_L23N_T3U_N9_PERSTN1_I2C_SDA_65		1.8 (LVCMOS18)
AE13	FPGA_TCK_PIN	TCK_0	TCK_0		1.8 (STARTUPE3)
AE15	FPGA_TDI	TDI_0	TDI_0		1.8 (STARTUPE3)
AC13	FPGA_TDO	TDO_0	TDO_0		1.8 (STARTUPE3)
AG15	FPGA_TMS	TMS_0	TMS_0		1.8 (STARTUPE3)
AN23	FPGA_USER_IN_0	IO_L20P_T3L_N2_AD1P_64	IO_L20P_T3L_N2_AD1P_64	SW1-1	1.8 (LVCMOS18)
AT22	GDISCRETE1_IN	IO_L16N_T2U_N7_QBC_AD3N_64	IO_L16N_T2U_N7_QBC_AD3N_64	P1.G1	1.8 (LVCMOS18)
AR23	GDISCRETE1_OUT	IO_L17P_T2U_N8_AD10P_64	IO_L17P_T2U_N8_AD10P_64		1.8 (LVCMOS18)
Y12	INIT_B_1V8	INIT_B_0	INIT_B_0		1.8 (STARTUPE3)
BC12	IPMB0_FPGA_SCL	IO_L7P_T1L_N0_QBC_AD13P_68	IO_L7P_T1L_N0_QBC_AD13P_68	P0.B5	1.8 (LVCMOS18)
BC11	IPMB0_FPGA_SDA	IO_L7N_T1L_N1_QBC_AD13N_68	IO_L7N_T1L_N1_QBC_AD13N_68	P0.A5	1.8 (LVCMOS18)
BB11	IPMB1_FPGA_SCL	IO_L8P_T1L_N2_AD5P_68	IO_L8P_T1L_N2_AD5P_68	P0.G4	1.8 (LVCMOS18)
BB10	IPMB1_FPGA_SDA	IO_L8N_T1L_N3_AD5N_68	IO_L8N_T1L_N3_AD5N_68	P0.F4	1.8 (LVCMOS18)
BC8	NVMRO_FPGA	IO_L9P_T1L_N4_AD12P_68	IO_L9P_T1L_N4_AD12P_68	P0.A4 (input only)	1.8 (LVCMOS18)
AN3	P1_0_RX_PIN_N	MGTYRXN0_226	MGTYRXN0_226	P1.B9	MGT
AN4	P1_0_RX_PIN_P	MGTYRXP0_226	MGTYRXP0_226	P1.A9	MGT
AN8	P1_0_TX_PIN_N	MGTYTXN0_226	MGTYTXN0_226	P1.E9	MGT
AN9	P1_0_TX_PIN_P	MGTYTXP0_226	MGTYTXP0_226	P1.D9	MGT
AM1	P1_1_RX_PIN_N	MGTYRXN1_226	MGTYRXN1_226	P1.C10	MGT
AM2	P1_1_RX_PIN_P	MGTYRXP1_226	MGTYRXP1_226	P1.B10	MGT
AM6	P1_1_TX_PIN_N	MGTYTXN1_226	MGTYTXN1_226	P1.F10	MGT
AM7	P1_1_TX_PIN_P	MGTYTXP1_226	MGTYTXP1_226	P1.E10	MGT
AL3	P1_2_RX_PIN_N	MGTYRXN2_226	MGTYRXN2_226	P1.B11	MGT
AL4	P1_2_RX_PIN_P	MGTYRXP2_226	MGTYRXP2_226	P1.A11	MGT
AL8	P1_2_TX_PIN_N	MGTYTXN2_226	MGTYTXN2_226	P1.E11	MGT
AL9	P1_2_TX_PIN_P	MGTYTXP2_226	MGTYTXP2_226	P1.D11	MGT
AK1	P1_3_RX_PIN_N	MGTYRXN3_226	MGTYRXN3_226	P1.C12	MGT
AK2	P1_3_RX_PIN_P	MGTYRXP3_226	MGTYRXP3_226	P1.B12	MGT
AK6	P1_3_TX_PIN_N	MGTYTXN3_226	MGTYTXN3_226	P1.F12	MGT

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AK7	P1_3_TX_PIN_P	MGTYTXP3_226	MGTYTXP3_226	P1.E12	MGT
AJ3	P1_4_RX_PIN_N	MGTYRXN0_227	MGTYRXN0_227	P1.B13	MGT
AJ4	P1_4_RX_PIN_P	MGTYRXP0_227	MGTYRXP0_227	P1.A13	MGT
AJ8	P1_4_TX_PIN_N	MGTYTXN0_227	MGTYTXN0_227	P1.E13	MGT
AJ9	P1_4_TX_PIN_P	MGTYTXP0_227	MGTYTXP0_227	P1.D13	MGT
AH1	P1_5_RX_PIN_N	MGTYRXN1_227	MGTYRXN1_227	P1.C14	MGT
AH2	P1_5_RX_PIN_P	MGTYRXP1_227	MGTYRXP1_227	P1.B14	MGT
AH6	P1_5_TX_PIN_N	MGTYTXN1_227	MGTYTXN1_227	P1.F14	MGT
AH7	P1_5_TX_PIN_P	MGTYTXP1_227	MGTYTXP1_227	P1.E14	MGT
AA3	P2_0_RX_PIN_N	MGTYRXN0_229	MGTYRXN0_229	P2.B1	MGT
AA4	P2_0_RX_PIN_P	MGTYRXP0_229	MGTYRXP0_229	P2.A1	MGT
AA8	P2_0_TX_PIN_N	MGTYTXN0_229	MGTYTXN0_229	P2.E1	MGT
AA9	P2_0_TX_PIN_P	MGTYTXP0_229	MGTYTXP0_229	P2.D1	MGT
Y1	P2_1_RX_PIN_N	MGTYRXN1_229	MGTYRXN1_229	P2.C2	MGT
Y2	P2_1_RX_PIN_P	MGTYRXP1_229	MGTYRXP1_229	P2.B2	MGT
Y6	P2_1_TX_PIN_N	MGTYTXN1_229	MGTYTXN1_229	P2.F2	MGT
Y7	P2_1_TX_PIN_P	MGTYTXP1_229	MGTYTXP1_229	P2.E2	MGT
L3	P2_10_RX_PIN_N	MGTYRXN2_231	MGTYRXN2_231	P2.B11	MGT
L4	P2_10_RX_PIN_P	MGTYRXP2_231	MGTYRXP2_231	P2.A11	MGT
L8	P2_10_TX_PIN_N	MGTYTXN2_231	MGTYTXN2_231	P2.E11	MGT
L9	P2_10_TX_PIN_P	MGTYTXP2_231	MGTYTXP2_231	P2.D11	MGT
K1	P2_11_RX_PIN_N	MGTYRXN3_231	MGTYRXN3_231	P2.C12	MGT
K2	P2_11_RX_PIN_P	MGTYRXP3_231	MGTYRXP3_231	P2.B12	MGT
K6	P2_11_TX_PIN_N	MGTYTXN3_231	MGTYTXN3_231	P2.F12	MGT
K7	P2_11_TX_PIN_P	MGTYTXP3_231	MGTYTXP3_231	P2.E12	MGT
J3	P2_12_RX_PIN_N	MGTYRXN0_232	MGTYRXN0_232	P2.B13	MGT
J4	P2_12_RX_PIN_P	MGTYRXP0_232	MGTYRXP0_232	P2.A13	MGT
J8	P2_12_TX_PIN_N	MGTYTXN0_232	MGTYTXN0_232	P2.E13	MGT
J9	P2_12_TX_PIN_P	MGTYTXP0_232	MGTYTXP0_232	P2.D13	MGT
H1	P2_13_RX_PIN_N	MGTYRXN1_232	MGTYRXN1_232	P2.C14	MGT
H2	P2_13_RX_PIN_P	MGTYRXP1_232	MGTYRXP1_232	P2.B14	MGT
H6	P2_13_TX_PIN_N	MGTYTXN1_232	MGTYTXN1_232	P2.F14	MGT
H7	P2_13_TX_PIN_P	MGTYTXP1_232	MGTYTXP1_232	P2.E14	MGT
G3	P2_14_RX_PIN_N	MGTYRXN2_232	MGTYRXN2_232	P2.B15	MGT
G4	P2_14_RX_PIN_P	MGTYRXP2_232	MGTYRXP2_232	P2.A15	MGT

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
G8	P2_14_TX_PIN_N	MGTYTXN2_232	MGTYTXN2_232	P2.E15	MGT
G9	P2_14_TX_PIN_P	MGTYTXP2_232	MGTYTXP2_232	P2.D15	MGT
F1	P2_15_RX_PIN_N	MGTYRXN3_232	MGTYRXN3_232	P2.C16	MGT
F2	P2_15_RX_PIN_P	MGTYRXP3_232	MGTYRXP3_232	P2.B16	MGT
F6	P2_15_TX_PIN_N	MGTYTXN3_232	MGTYTXN3_232	P2.F16	MGT
F7	P2_15_TX_PIN_P	MGTYTXP3_232	MGTYTXP3_232	P2.E16	MGT
W3	P2_2_RX_PIN_N	MGTYRXN2_229	MGTYRXN2_229	P2.B3	MGT
W4	P2_2_RX_PIN_P	MGTYRXP2_229	MGTYRXP2_229	P2.A3	MGT
W8	P2_2_TX_PIN_N	MGTYTXN2_229	MGTYTXN2_229	P2.E3	MGT
W9	P2_2_TX_PIN_P	MGTYTXP2_229	MGTYTXP2_229	P2.D3	MGT
V1	P2_3_RX_PIN_N	MGTYRXN3_229	MGTYRXN3_229	P2.C4	MGT
V2	P2_3_RX_PIN_P	MGTYRXP3_229	MGTYRXP3_229	P2.B4	MGT
V6	P2_3_TX_PIN_N	MGTYTXN3_229	MGTYTXN3_229	P2.F4	MGT
V7	P2_3_TX_PIN_P	MGTYTXP3_229	MGTYTXP3_229	P2.E4	MGT
U3	P2_4_RX_PIN_N	MGTYRXN0_230	MGTYRXN0_230	P2.B5	MGT
U4	P2_4_RX_PIN_P	MGTYRXP0_230	MGTYRXP0_230	P2.A5	MGT
U8	P2_4_TX_PIN_N	MGTYTXN0_230	MGTYTXN0_230	P2.E5	MGT
U9	P2_4_TX_PIN_P	MGTYTXP0_230	MGTYTXP0_230	P2.D5	MGT
T1	P2_5_RX_PIN_N	MGTYRXN1_230	MGTYRXN1_230	P2.C6	MGT
T2	P2_5_RX_PIN_P	MGTYRXP1_230	MGTYRXP1_230	P2.B6	MGT
T6	P2_5_TX_PIN_N	MGTYTXN1_230	MGTYTXN1_230	P2.F6	MGT
T7	P2_5_TX_PIN_P	MGTYTXP1_230	MGTYTXP1_230	P2.E6	MGT
R3	P2_6_RX_PIN_N	MGTYRXN2_230	MGTYRXN2_230	P2.B7	MGT
R4	P2_6_RX_PIN_P	MGTYRXP2_230	MGTYRXP2_230	P2.A7	MGT
R8	P2_6_TX_PIN_N	MGTYTXN2_230	MGTYTXN2_230	P2.E7	MGT
R9	P2_6_TX_PIN_P	MGTYTXP2_230	MGTYTXP2_230	P2.D7	MGT
P1	P2_7_RX_PIN_N	MGTYRXN3_230	MGTYRXN3_230	P2.C8	MGT
P2	P2_7_RX_PIN_P	MGTYRXP3_230	MGTYRXP3_230	P2.B8	MGT
P6	P2_7_TX_PIN_N	MGTYTXN3_230	MGTYTXN3_230	P2.F8	MGT
P7	P2_7_TX_PIN_P	MGTYTXP3_230	MGTYTXP3_230	P2.E8	MGT
N3	P2_8_RX_PIN_N	MGTYRXN0_231	MGTYRXN0_231	P2.B9	MGT
N4	P2_8_RX_PIN_P	MGTYRXP0_231	MGTYRXP0_231	P2.A9	MGT
N8	P2_8_TX_PIN_N	MGTYTXN0_231	MGTYTXN0_231	P2.E9	MGT
N9	P2_8_TX_PIN_P	MGTYTXP0_231	MGTYTXP0_231	P2.D9	MGT
M1	P2_9_RX_PIN_N	MGTYRXN1_231	MGTYRXN1_231	P2.C10	MGT

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
M2	P2_9_RX_PIN_P	MGTYRXP1_231	MGTYRXP1_231	P2.B10	MGT
M6	P2_9_TX_PIN_N	MGTYTXN1_231	MGTYTXN1_231	P2.F10	MGT
M7	P2_9_TX_PIN_P	MGTYTXP1_231	MGTYTXP1_231	P2.E10	MGT
AP21	P2_GPIO_EN_L	IO_T3U_N12_64	IO_T3U_N12_64		1.8 (LVCMOS18)
BD24	P2_GPIO_G1_1V8	IO_L3N_T0L_N5_AD15N_64	IO_L3N_T0L_N5_AD15N_64	P2.G1	1.8 (LVCMOS18)
AN24	P2_GPIO_G1_DIR	IO_L21P_T3L_N4_AD8P_64	IO_L21P_T3L_N4_AD8P_64		1.8 (LVCMOS18)
BD20	P2_GPIO_G11_1V8	IO_L6P_T0U_N10_AD6P_64	IO_L6P_T0U_N10_AD6P_64	P2.G11	1.8 (LVCMOS18)
AM22	P2_GPIO_G11_DIR	IO_L23N_T3U_N9_64	IO_L23N_T3U_N9_64		1.8 (LVCMOS18)
BE20	P2_GPIO_G13_1V8	IO_L6N_T0U_N11_AD6N_64	IO_L6N_T0U_N11_AD6N_64	P2.G13	1.8 (LVCMOS18)
AL21	P2_GPIO_G13_DIR	IO_L24P_T3U_N10_64	IO_L24P_T3U_N10_64		1.8 (LVCMOS18)
BF20	P2_GPIO_G15_1V8	IO_T0U_N12_VRP_64	IO_T0U_N12_VRP_64	P2.G15	1.8 (LVCMOS18)
AM21	P2_GPIO_G15_DIR	IO_L24N_T3U_N11_64	IO_L24N_T3U_N11_64		1.8 (LVCMOS18)
BE22	P2_GPIO_G3_1V8	IO_L4P_T0U_N6_DBC_-AD7P_64	IO_L4P_T0U_N6_DBC_-AD7P_64	P2.G3	1.8 (LVCMOS18)
AP24	P2_GPIO_G3_DIR	IO_L21N_T3L_N5_AD8N_64	IO_L21N_T3L_N5_AD8N_64		1.8 (LVCMOS18)
BF22	P2_GPIO_G5_1V8	IO_L4N_T0U_N7_DBC_-AD7N_64	IO_L4N_T0U_N7_DBC_-AD7N_64	P2.G5	1.8 (LVCMOS18)
AL24	P2_GPIO_G5_DIR	IO_L22P_T3U_N6_DBC-_AD0P_64	IO_L22P_T3U_N6_DBC-_AD0P_64		1.8 (LVCMOS18)
BD21	P2_GPIO_G7_1V8	IO_L5P_T0U_N8_AD14P_64	IO_L5P_T0U_N8_AD14P_64	P2.G7	1.8 (LVCMOS18)
AM24	P2_GPIO_G7_DIR	IO_L22N_T3U_N7_DBC-_AD0N_64	IO_L22N_T3U_N7_DBC-_AD0N_64		1.8 (LVCMOS18)
BE21	P2_GPIO_G9_1V8	IO_L5N_T0U_N9_AD14N_64	IO_L5N_T0U_N9_AD14N_64	P2.G9	1.8 (LVCMOS18)
AL22	P2_GPIO_G9_DIR	IO_L23P_T3U_N8_64	IO_L23P_T3U_N8_64		1.8 (LVCMOS18)
BC1	PCIE_RX0_PIN_N	MGTYRXN0_224	MGTYRXN0_224	P1.B1	MGT
BC2	PCIE_RX0_PIN_P	MGTYRXP0_224	MGTYRXP0_224	P1.A1	MGT
BA1	PCIE_RX1_PIN_N	MGTYRXN1_224	MGTYRXN1_224	P1.C2	MGT
BA2	PCIE_RX1_PIN_P	MGTYRXP1_224	MGTYRXP1_224	P1.B2	MGT
AW3	PCIE_RX2_PIN_N	MGTYRXN2_224	MGTYRXN2_224	P1.B3	MGT
AW4	PCIE_RX2_PIN_P	MGTYRXP2_224	MGTYRXP2_224	P1.A3	MGT
AV1	PCIE_RX3_PIN_N	MGTYRXN3_224	MGTYRXN3_224	P1.C4	MGT
AV2	PCIE_RX3_PIN_P	MGTYRXP3_224	MGTYRXP3_224	P1.B4	MGT
AU3	PCIE_RX4_PIN_N	MGTYRXN0_225	MGTYRXN0_225	P1.B5	MGT
AU4	PCIE_RX4_PIN_P	MGTYRXP0_225	MGTYRXP0_225	P1.A5	MGT
AT1	PCIE_RX5_PIN_N	MGTYRXN1_225	MGTYRXN1_225	P1.C6	MGT
AT2	PCIE_RX5_PIN_P	MGTYRXP1_225	MGTYRXP1_225	P1.B6	MGT

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AR3	PCIE_RX6_PIN_N	MGTYRXN2_225	MGTYRXN2_225	P1.B7	MGT
AR4	PCIE_RX6_PIN_P	MGTYRXP2_225	MGTYRXP2_225	P1.A7	MGT
AP1	PCIE_RX7_PIN_N	MGTYRXN3_225	MGTYRXN3_225	P1.C8	MGT
AP2	PCIE_RX7_PIN_P	MGTYRXP3_225	MGTYRXP3_225	P1.B8	MGT
BF4	PCIE_TX0_PIN_N	MGTYTXN0_224	MGTYTXN0_224	P1.E1	MGT
BF5	PCIE_TX0_PIN_P	MGTYTXP0_224	MGTYTXP0_224	P1.D1	MGT
BD4	PCIE_TX1_PIN_N	MGTYTXN1_224	MGTYTXN1_224	P1.F2	MGT
BD5	PCIE_TX1_PIN_P	MGTYTXP1_224	MGTYTXP1_224	P1.E2	MGT
BB4	PCIE_TX2_PIN_N	MGTYTXN2_224	MGTYTXN2_224	P1.E3	MGT
BB5	PCIE_TX2_PIN_P	MGTYTXP2_224	MGTYTXP2_224	P1.D3	MGT
AV6	PCIE_TX3_PIN_N	MGTYTXN3_224	MGTYTXN3_224	P1.F4	MGT
AV7	PCIE_TX3_PIN_P	MGTYTXP3_224	MGTYTXP3_224	P1.E4	MGT
AU8	PCIE_TX4_PIN_N	MGTYTXN0_225	MGTYTXN0_225	P1.E5	MGT
AU9	PCIE_TX4_PIN_P	MGTYTXP0_225	MGTYTXP0_225	P1.D5	MGT
AT6	PCIE_TX5_PIN_N	MGTYTXN1_225	MGTYTXN1_225	P1.F6	MGT
AT7	PCIE_TX5_PIN_P	MGTYTXP1_225	MGTYTXP1_225	P1.E6	MGT
AR8	PCIE_TX6_PIN_N	MGTYTXN2_225	MGTYTXN2_225	P1.E7	MGT
AR9	PCIE_TX6_PIN_P	MGTYTXP2_225	MGTYTXP2_225	P1.D7	MGT
AP6	PCIE_TX7_PIN_N	MGTYTXN3_225	MGTYTXN3_225	P1.F8	MGT
AP7	PCIE_TX7_PIN_P	MGTYTXP3_225	MGTYTXP3_225	P1.E8	MGT
AR26	PERSTN0	IO_T3U_N12_PERSTN0_65	IO_T3U_N12_PERSTN0_65	P1.G15 or P0.B4	1.2 (LVCMOS12)
AD12	POR_OVERRIDE	POR_OVERRIDE	POR_OVERRIDE		NA
AC37	PROGCLK0_0_PIN_N	MGTREFCLK0N_125	MGTREFCLK0N_129		MGT REFCLK
AC36	PROGCLK0_0_PIN_P	MGTREFCLK0P_125	MGTREFCLK0P_129		MGT REFCLK
AG37	PROGCLK0_1_PIN_N	MGTREFCLK0N_124	MGTREFCLK0N_128		MGT REFCLK
AG36	PROGCLK0_1_PIN_P	MGTREFCLK0P_124	MGTREFCLK0P_128		MGT REFCLK
H10	PROGCLK0_2_PIN_N	MGTREFCLK0N_232	MGTREFCLK0N_232		MGT REFCLK
H11	PROGCLK0_2_PIN_P	MGTREFCLK0P_232	MGTREFCLK0P_232		MGT REFCLK
M10	PROGCLK0_3_PIN_N	MGTREFCLK0N_231	MGTREFCLK0N_231		MGT REFCLK
M11	PROGCLK0_3_PIN_P	MGTREFCLK0P_231	MGTREFCLK0P_231		MGT REFCLK

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
T10	PROGCLK0_4_PIN_N	MGTREFCLK0N_230	MGTREFCLK0N_230		MGT REFCLK
T11	PROGCLK0_4_PIN_P	MGTREFCLK0P_230	MGTREFCLK0P_230		MGT REFCLK
Y10	PROGCLK0_5_PIN_N	MGTREFCLK0N_229	MGTREFCLK0N_229		MGT REFCLK
Y11	PROGCLK0_5_PIN_P	MGTREFCLK0P_229	MGTREFCLK0P_229		MGT REFCLK
AH10	PROGCLK0_6_PIN_N	MGTREFCLK0N_227	MGTREFCLK0N_227		MGT REFCLK
AH11	PROGCLK0_6_PIN_P	MGTREFCLK0P_227	MGTREFCLK0P_227		MGT REFCLK
AM10	PROGCLK0_7_PIN_N	MGTREFCLK0N_226	MGTREFCLK0N_226		MGT REFCLK
AM11	PROGCLK0_7_PIN_P	MGTREFCLK0P_226	MGTREFCLK0P_226		MGT REFCLK
AT10	PROGCLK0_8_PIN_N	MGTREFCLK0N_225	MGTREFCLK0N_225		MGT REFCLK
AT11	PROGCLK0_8_PIN_P	MGTREFCLK0P_225	MGTREFCLK0P_225		MGT REFCLK
BC9	PROGCLK0_9_N	IO_L11N_T1U_N9_GC_68	IO_L11N_T1U_N9_GC_68		1.8 (LVDS with DIFF_TERM_ADV)
BB9	PROGCLK0_9_P	IO_L11P_T1U_N8_GC_68	IO_L11P_T1U_N8_GC_68		1.8 (LVDS with DIFF_TERM_ADV)
AA37	PROGCLK1_0_PIN_N	MGTREFCLK1N_125	MGTREFCLK1N_129		MGT REFCLK
AA36	PROGCLK1_0_PIN_P	MGTREFCLK1P_125	MGTREFCLK1P_129		MGT REFCLK
AE37	PROGCLK1_1_PIN_N	MGTREFCLK1N_124	MGTREFCLK1N_128		MGT REFCLK
AE36	PROGCLK1_1_PIN_P	MGTREFCLK1P_124	MGTREFCLK1P_128		MGT REFCLK
F10	PROGCLK1_2_PIN_N	MGTREFCLK1N_232	MGTREFCLK1N_232		MGT REFCLK
F11	PROGCLK1_2_PIN_P	MGTREFCLK1P_232	MGTREFCLK1P_232		MGT REFCLK
K10	PROGCLK1_3_PIN_N	MGTREFCLK1N_231	MGTREFCLK1N_231		MGT REFCLK
K11	PROGCLK1_3_PIN_P	MGTREFCLK1P_231	MGTREFCLK1P_231		MGT REFCLK
P10	PROGCLK1_4_PIN_N	MGTREFCLK1N_230	MGTREFCLK1N_230		MGT REFCLK
P11	PROGCLK1_4_PIN_P	MGTREFCLK1P_230	MGTREFCLK1P_230		MGT REFCLK
V10	PROGCLK1_5_PIN_N	MGTREFCLK1N_229	MGTREFCLK1N_229		MGT REFCLK
V11	PROGCLK1_5_PIN_P	MGTREFCLK1P_229	MGTREFCLK1P_229		MGT REFCLK
AF10	PROGCLK1_6_PIN_N	MGTREFCLK1N_227	MGTREFCLK1N_227		MGT REFCLK

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
AF11	PROGCLK1_6_PIN_P	MGTREFCLK1P_227	MGTREFCLK1P_227		MGT REFCLK
AK10	PROGCLK1_7_PIN_N	MGTREFCLK1N_226	MGTREFCLK1N_226		MGT REFCLK
AK11	PROGCLK1_7_PIN_P	MGTREFCLK1P_226	MGTREFCLK1P_226		MGT REFCLK
AP10	PROGCLK1_8_PIN_N	MGTREFCLK1N_225	MGTREFCLK1N_225		MGT REFCLK
AP11	PROGCLK1_8_PIN_P	MGTREFCLK1P_225	MGTREFCLK1P_225		MGT REFCLK
AV10	PROGCLK1_9_PIN_N	MGTREFCLK1N_224	MGTREFCLK1N_224		MGT REFCLK
AV11	PROGCLK1_9_PIN_P	MGTREFCLK1P_224	MGTREFCLK1P_224		MGT REFCLK
AE12	PROGRAM_B_1V8	PROGRAM_B_0	PROGRAM_B_0		1.8 (STARTUPE3)
AA12	PUDC	PUDC_B_0	PUDC_B_0		1.8 (STARTUPE3)
BA22	REFCLK_OUT_EN_1V8	IO_L11N_T1U_N9_GC_64	IO_L11N_T1U_N9_GC_64		1.8 (LVCMOS18)
AW8	REFCLK_PIN_N	MGTREFCLK0N_224	MGTREFCLK0N_224	P0.F8	MGT REFCLK
AW9	REFCLK_PIN_P	MGTREFCLK0P_224	MGTREFCLK0P_224	P0.E8	MGT REFCLK
AW30	REFCLK300M_0_PIN_N	IO_L13N_T2L_N1_GC_QBC_40	IO_L13N_T2L_N1_GC_QBC_61		1.2
AW29	REFCLK300M_0_PIN_P	IO_L13P_T2L_N0_GC_QBC_40	IO_L13P_T2L_N0_GC_QBC_61		1.2
AW26	REFCLK300M_1_PIN_N	IO_L13N_T2L_N1_GC_QBC_A07_D23_65	IO_L13N_T2L_N1_GC_QBC_A07_D23_65		1.2
AV26	REFCLK300M_1_PIN_P	IO_L13P_T2L_N0_GC_QBC_A06_D22_65	IO_L13P_T2L_N0_GC_QBC_A06_D22_65		1.2
H26	REFCLK300M_2_PIN_N	IO_L13N_T2L_N1_GC_QBC_48	IO_L13N_T2L_N1_GC_QBC_71		1.2
J26	REFCLK300M_2_PIN_P	IO_L13P_T2L_N0_GC_QBC_48	IO_L13P_T2L_N0_GC_QBC_71		1.2
G24	REFCLK300M_3_PIN_N	IO_L13N_T2L_N1_GC_QBC_72	IO_L13N_T2L_N1_GC_QBC_74		1.2
G25	REFCLK300M_3_PIN_P	IO_L13P_T2L_N0_GC_QBC_72	IO_L13P_T2L_N0_GC_QBC_74		1.2
BD23	RS232_0_RX_1V8	IO_L2P_T0L_N2_64	IO_L2P_T0L_N2_64	P1.G11	1.8 (LVCMOS18)
BF23	RS232_0_TX_1V8	IO_L1N_T0L_N1_DBC_64	IO_L1N_T0L_N1_DBC_64	P1.G9	1.8 (LVCMOS18)
BC24	RS232_1_RX_1V8	IO_L3P_T0L_N4_AD15P_64	IO_L3P_T0L_N4_AD15P_64	P2.G3	1.8 (LVCMOS18)
BE23	RS232_1_TX_1V8	IO_L2N_T0L_N3_64	IO_L2N_T0L_N3_64	P2.G1	1.8 (LVCMOS18)
AV23	SE_REFCLK_OUT_1V8	IO_L13P_T2L_N0_GC_QBC_64	IO_L13P_T2L_N0_GC_QBC_64	P0.F8 - P0.E8	1.8 (LVCMOS18)

Table 7 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	VU9P Pin Name	VU13P Pin Name	External Connector	Bank Voltage
BD9	SPARE_SCL	IO_L6P_T0U_N10_AD6P_68	IO_L6P_T0U_N10_AD6P_68		1.8 (LVCMOS18)
BD8	SPARE_SDA	IO_L6N_T0U_N11_AD6N_68	IO_L6N_T0U_N11_AD6N_68		1.8 (LVCMOS18)
BD10	SPARE_WP	IO_T0U_N12_VRP_68	IO_T0U_N12_VRP_68		1.8 (LVCMOS18)
BD11	SRVC_MD_1V8_L	IO_T1U_N12_68	IO_T1U_N12_68		SW1-2
AV22	SYSCON_1V8_L	IO_L15N_T2L_N5_AD11N_64	IO_L15N_T2L_N5_AD11N_64	P1.G5	1.8 (LVCMOS18)
AR22	SYSRESET_OUT_L	IO_L16P_T2U_N6_QBC-_AD3P_64	IO_L16P_T2U_N6_QBC-_AD3P_64		1.8 (LVCMOS18)
BF24	UART_0_RX_1V8	IO_L1P_T0L_N0_DBC_64	IO_L1P_T0L_N0_DBC_64	P1.G11	1.8 (LVCMOS18)
AP23	UART_0_TX_1V8	IO_L20N_T3L_N3_AD1N_64	IO_L20N_T3L_N3_AD1N_64	P1.G9	1.8 (LVCMOS18)
BA20	USER_LED_0_1V8	IO_L7P_T1L_N0_QBC_-AD13P_64	IO_L7P_T1L_N0_QBC_-AD13P_64		1.8 (LVCMOS18)
BB20	USER_LED_1_1V8	IO_L7N_T1L_N1_QBC_-AD13N_64	IO_L7N_T1L_N1_QBC_-AD13N_64		1.8 (LVCMOS18)
BB21	USER_LED_2_1V8	IO_L8P_T1L_N2_AD5P_64	IO_L8P_T1L_N2_AD5P_64		1.8 (LVCMOS18)
BC21	USER_LED_3_1V8	IO_L8N_T1L_N3_AD5N_64	IO_L8N_T1L_N3_AD5N_64		1.8 (LVCMOS18)
BB22	USER_LED_4_1V8	IO_L9P_T1L_N4_AD12P_64	IO_L9P_T1L_N4_AD12P_64		1.8 (LVCMOS18)
BC22	USER_LED_5_1V8	IO_L9N_T1L_N5_AD12N_64	IO_L9N_T1L_N5_AD12N_64		1.8 (LVCMOS18)
BA24	USER_LED_6_1V8	IO_L10P_T1U_N6_QBC-_AD4P_64	IO_L10P_T1U_N6_QBC-_AD4P_64		1.8 (LVCMOS18)
BB24	USER_LED_7_1V8	IO_L10N_T1U_N7_QBC-_AD4N_64	IO_L10N_T1U_N7_QBC-_AD4N_64		1.8 (LVCMOS18)

Table 7 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
28 May 2020	0.1	K. Roth	Pre-release Draft
1 Jun 2020	0.2	K. Roth	Modified QSPI descriptions to use x4 interface (not x8) in Configuration From Flash Memory
6 Oct 2020	1.0	K. Roth	Added diagram for VU9P in Functional Description, updated images with product photos, added weight to Physical Specifications, updated frequency specified for PROGCLK0 to 100MHz in PROGCLK0 Clock, added text to LEDs stating that LEDs can flicker when unconstrained or FPGA is unconfigured.
7 Oct 2020	1.1	K. Roth	Corrected bank arrows on block diagrams in section Functional Description, added note about clamshell for DDR4 SDRAM, added vibration testing for FireFly
13 Oct 2020	1.2	K. Roth	Removed 'G' from LED names and re-ordered LED references in table within LEDs, added VU9P pin names to pinout table.
14 Jan 2022	1.3	K. Roth	Corrected DDR4 part number listed in section DDR4 SDRAM, added conduction cooled thermal efficiency into section Thermal Performance.
28 Jul 2022	1.4	K. Roth	Corrected arrows and cross-hatch MGT blocks on block diagrams in section Functional Description.
31 Dec 2024	1.5	K. Roth	Updated clock diagram to show the correct DIP switch index for CLK_SEL control.

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